Panasonic®

PROGRAMMABLE CONTROLLER

FP2 High-speed Counter Unit
FP2 Pulse I/O Unit
Manual

ARCT1F323E-4

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Safety Precautions

Observe the following notices to ensure personal safety or to prevent accidents.
To ensure that you use this product correctly, read this User's Manual thoroughly before use.
Make sure that you fully understand the product and information on safety.
This manual uses two safety flags to indicate different levels of danger.

WARNING

If critical situations that could lead to user's death or serious injury is assumed by mishandling of the product.

-Always take precautions to ensure the overall safety of your system, so that the whole system remains safe in the event of failure of this product or other external factor.
-Do not use this product in areas with inflammable gas. It could lead to an explosion.
-Exposing this product to excessive heat or open flames could cause damage to the lithium battery or other electronic parts.

CAUTION

If critical situations that could lead to user's injury or only property damage is assumed by mishandling of the product.

-To prevent excessive exothermic heat or smoke generation, use this product at the values less than the maximum of the characteristics and performance that are assured in these specifications.
-Do not dismantle or remodel the product. It could cause excessive exothermic heat or smoke generation.
-Do not touch the terminal while turning on electricity. It could lead to an electric shock.
-Use the external devices to function the emergency stop and interlock circuit.
-Connect the wires or connectors securely.
The loose connection could cause excessive exothermic heat or smoke generation.
-Do not allow foreign matters such as liquid, flammable materials, metals to go into the inside of the product. It could cause excessive exothermic heat or smoke generation.
-Do not undertake construction (such as connection and disconnection) while the power supply is on. It could lead to an electric shock.

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Interchangeability With the FP3 High−speed Counter Unit

The FP2 and FP3 High−speed Counter Units are not compatible in terms of either hardware or software. Also, programs cannot be used interchangeably.

Comparison with the FP3 High−speed Counter Unit

Comparison item		FP2 High−speed Counter Unit	FP3 High−speed Counter Unit
High−speed counter	**No. of channels**	4 channels	1 or 2 channels (separate product numbers)
	Max. calculation speed	200 kHz max.	100 kHz max.
	Compared output	Can be set to any of 8 target values.	Separate target value areas for the two channels.
Input time constant		Can be set separately for the two inputs. − 4 µs − 8 µs − 16 µs − 32 µs	Can be set separately for each unit. − 5 µs − 10 µs − 20 µs − 62.5 µs
Interrupt function		Up to 8 points per unit. Interrupt programs can be booted in either of the following cases. − When matching high−speed counter target values − When external input is used	Only 1 point per unit. Interrupt program can be booted only when matching high−speed counter target values.
External connections		Connector (40−pin)	Terminal block

Chapter 1

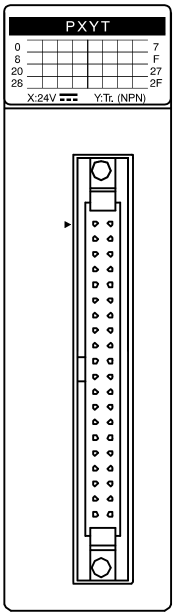
Functions of the Unit

1.1 Features and Functions of the Unit

1.1.1 Features of the Unit

The FP2 High−speed Counter Unit and FP2 Pulse I/O Unit are the intelligent unit that can be installed in the FP2 programmable controller to enable easy access to high−speed counter functions. The principle features of the various units are as described below.

In addition to a high−speed counter function, the unit also includes many convenient functions like those listed below.



Operates as an input/output mixing unit.	Normal I/O function (see Chapter 5)
Sets the effective pulse width for input signals.	Input time constant functions (see Chapter 6)
Generates interrupt signals.	Interrupt function (see Chapter 7)
Counts the number of pulses.	Counter function (see Chapter 8)
Compares the number of pulses to a set value and outputs the result.	Output comparison function (see Chapter 9)
Outputs pulses.	Pulse output function (FP2 Pulse I/O unit only) (see Chapter 10)
Outputs PWM.	PWM output function (FP2 Pulse I/O unit only) (see Chapter 11)

The pulse output function and PWM output function are available only with the pulse I/O unit. Please be aware that these cannot be used with the high−speed counter unit.

Streamlined system configuration free of waste

Of the I/O terminals on the unit, whichever terminal have not been allocated to functions can be used as ordinary I/O terminals. This makes it possible to configure a streamlined system with no waste, and enables the counter function, sensor input, and other functions to be carried out using a single FP2 High−speed Counter Unit or FP2 Pulse I/O Unit.

Interrupt function provided

In addition to interrupt control based on ordinary external input, interrupt control based on matching the counter elapsed value is also supported.

☛ next page

Easy positioning control with a single FP2 pulse I/O unit

The FP2 Pulse I/O Unit is equipped with a pulse output function. Output pulses can be fed back to the unit, allowing easy positioning control with a single unit.

Four 0.8 A outputs provided

1.1.2 Unit Product Numbers

Name	Specifications	Built−in functions	Parts No.
FP2 High−speed Counter Unit (NPN output)	Input: 24 VDC + common Output: NPN 5 to 24 VDC (0.1 A 12 points/0.8 A 4 points)	8 interrupt inputs 4−channel high−speed counter 8 comparison outputs	FP2−HSCT
FP2 High−speed Counter Unit (PNP output)	Input: 24 VDC − common Output: PNP 5 to 24 VDC (0.1 A 12 points/0.8 A 4 points)		FP2−HSCP
FP2 Pulse I/O Unit (NPN output)	Input: 24 VDC + common Output: NPN 5 to 24 VDC (0.1 A 12 points/0.8 A 4 points)	8 interrupt inputs 4−channel high−speed counter 8 comparison outputs 4 pulse output channels 4 PWM output channels	FP2−PXYT
FP2 Pulse I/O Unit (PNP output)	Input: 24 VDC − common Output: PNP 5 to 24 VDC (0.1 A 12 points/0.8 A 4 points)		FP2−PXYP

Note: The unit comes with one 40−pin Wire−pressed terminal type connector.

Maintenance parts

Name	Contents	Product No.
Wire−pressed terminal type connector set	two pieces (40−pin, with semi−cover, AWG22, 24)	AFP2801

Note

When using the FP2 High−Speed Counter/Pulse I/O Unit, the FP2 CPU unit used should be Ver. 1.09 or a subsequent version.

1.2 Unit Functions and How They Work

The various functions are operated by entering settings in the shared memory. The interrupt function mode is set using the mode setting switches on the side panel of the main unit.

When the unit is shipped from the factory, all of the switches are set to the “off” position (no interrupt function). When the power supply is turned on, the unit functions as an ordinary I/O unit.

1.2.1 Ordinary I/O Functions

The FP2 High−speed Counter Unit and FP2 Pulse I/O Unit operates as a 32−input, 32−output mixed input/output unit in its default state, when none of the mode setting switches on the side panel or the shared memory settings have been changed. Because the first 16 inputs and the first 16 outputs are allocated to terminals, however, in practical terms the unit functions as a mixed input/output unit with 16 inputs and 16 outputs.

The I/O allocations change depending on the position in which the unit is installed.
For example, if the unit is installed in slot 0, the dedicated I/Os will be WX0 to 1 and WY2 to 3. WX0 and WY2 are actually allocated to the terminals.

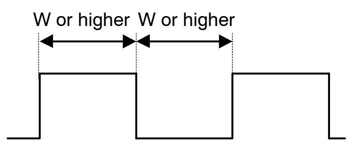
When other functions are being used, the inputs and outputs of those functions are given priority, but those inputs and outputs that have not been allocated to functions are available for use.

1.2.2 Input Time Constant Function

The input time constant function specifies the effective pulse width in response to input signals from an input/output connector. Input signals below the effective pulse width are judged to be noise.

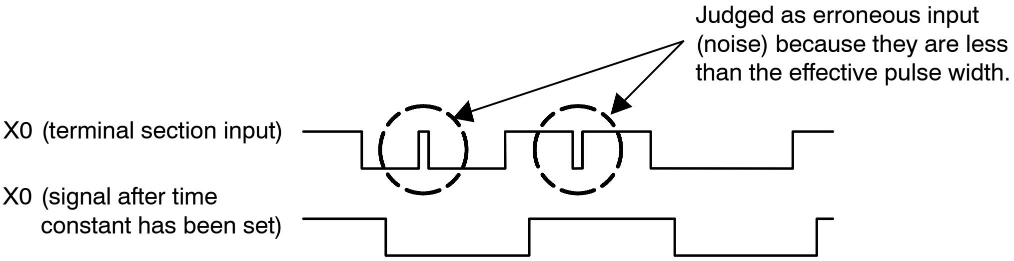
Four constants can be specified as the effective pulse width, two for each input/output connector, as indicated below.

Effective pulse width W μs	Max. calculation speed
No setting	200 kHz
4	125 kHz
8	62.5 kHz
16	31.2 kHz
32	15.6 kHz



Setting unit	External input terminal
Group 1	A1, A2 (input allocation X0, X1)
Group 2	A3, A4 (input allocation X2, X3)
Group 3	A5, A6 (input allocation X4, X5)
Group 4	A7, A8 (input allocation X6, X7)
Group 5	B1, B2 (input allocation X8, X9)
Group 6	B3, B4 (input allocation XA, XB)
Group 7	B5, B6 (input allocation XC, XD)
Group 8	B7, B8 (input allocation XE, XF)

With the input time constant function, the effective pulse width of the input signal can be specified, which effectively prevents erroneous input in environments with high noise levels. For detailed information on settings, please see page 6 – 3, “Input time constant function”.



☞ **Note**

The time constant function is set to “No setting” in the default settings.

1.2.3 Interrupt Function

The interrupt function is set to the following modes based on the status of the mode setting switches when the power supply is turned on.

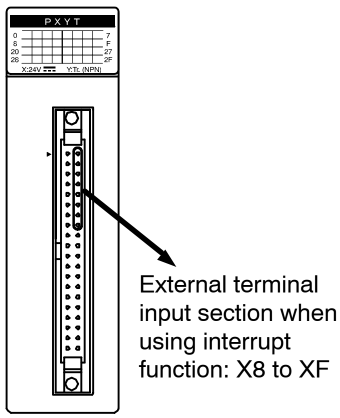
Mode	Unit operation	No. of interrupts available	Interrupt program no. that can be set in program	Interrupt input *3
A	Unit without interrupt function	0	—	—
B	Unit with interrupt function	8	INT0 to 7 or INT8 to 15 *1	– I/O connectors (X8 to XF) – Comparison matching signal (EQ0 to EQ7) *2
C	Intelligent unit that generate interrupts	1	INT16 to 23 *1	– I/O connectors (X8) – Comparison matching signal (EQ0) *2

*1: The applicable interrupt program numbers vary depending on the position at which the unit is installed.
*2: This is an internal signal for the comparison function. It is generated if the counter elapsed value matches the comparison value.
*3: The input signal used to generate the interrupt can be selected. (I/O connector or comparison matching signal)

Example:

Correspondence between ladder command and interrupt signal

Mode B	Mode C
INT0 ← X8, or EQ0	INT16 ← X8, or EQ0
INT1 ← X9, or EQ1	
INT2 ← XA, or EQ2	
INT3 ← XB, or EQ3	
INT4 ← XC, or EQ4	
INT5 ← XD, or EQ5	
INT6 ← XE, or EQ6	
INT7 ← XF, or EQ7	



Interrupts are generated at the timing at which edges are input.

External terminal input

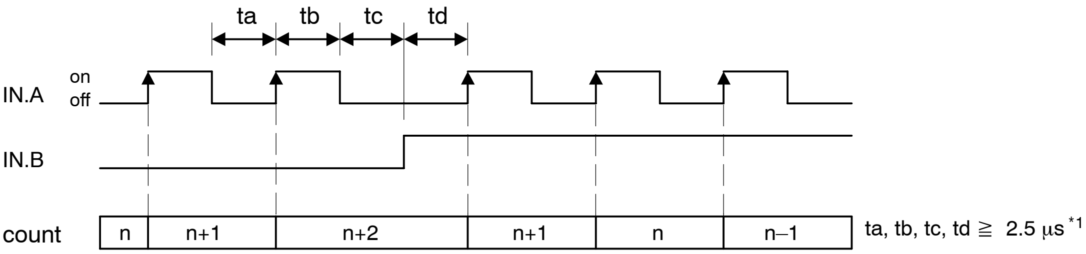
Comparison matching signal input

1.2.4 Counter Function

The FP2 High−speed Counter Unit and FP2 Pulse I/O Unit are equipped with four counter channels, and counting is carried out in the three input modes described below. The input modes can be set separately for each of the channels.

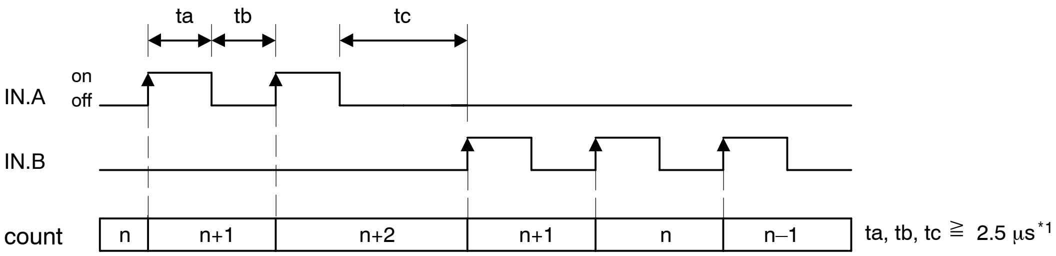
Direction control

The count value is incremented or decremented based on the pulse train and the direction signal.



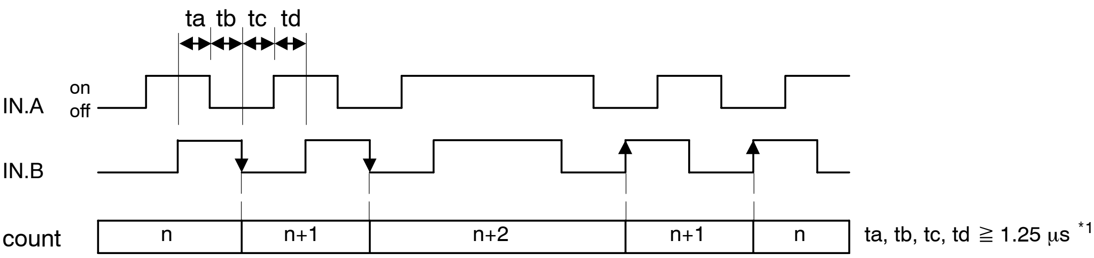
Individual input

The count value is incremented or decremented based on the CW and CCW input signals.



Phase different

The count value is incremented or decremented based on the phase differential input of the encoder or another device.

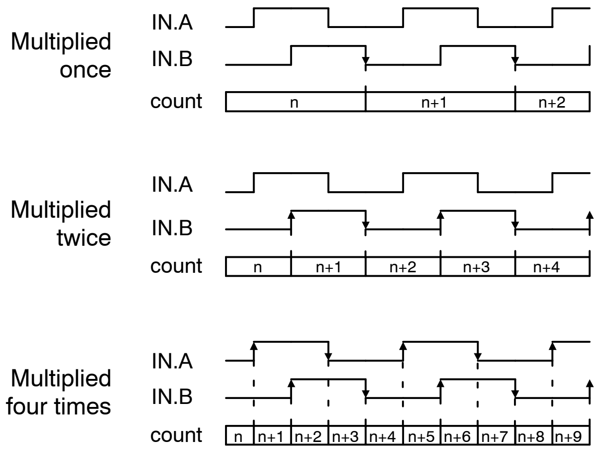


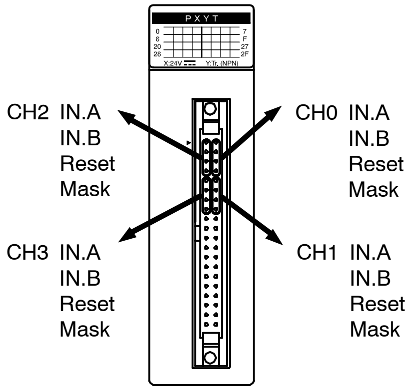
*1: This is the value when “No setting” is set for the input time constant function.

Tip

Doubling multiplier function

The phase differential input mode has the three doubling functions noted below.



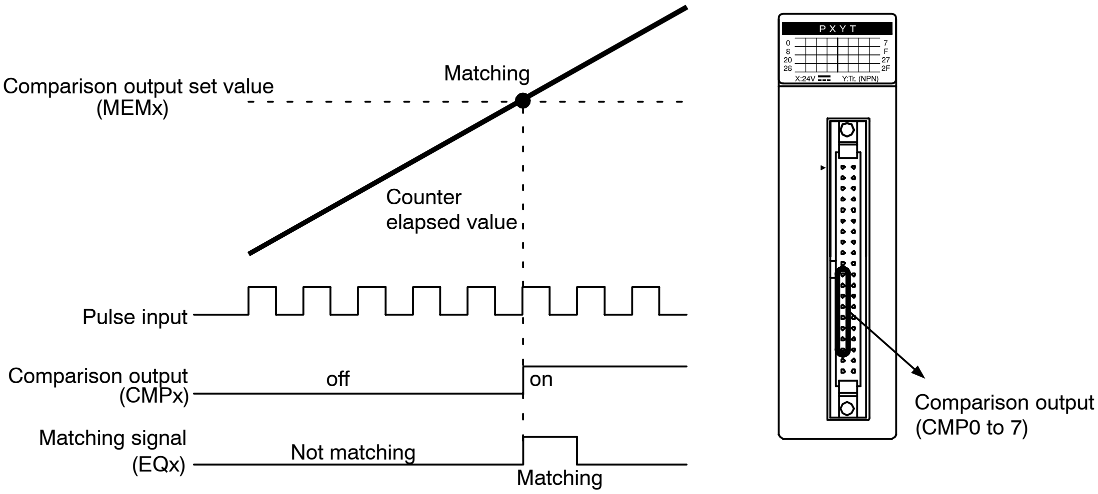


1.2.5 Comparison Output Function

The FP2 High−speed Counter Unit and FP2 Pulse I/O Unit are equipped with eight comparison outputs (CMP0 to CMP7).

The comparison outputs are output as a result of the counter elapsed value and the comparison output set value being compared.
The comparison output set values are specified in the shared memory (MEM0 to MEM7).

Counter elapsed value < Comparison output set value → Comparison output: off
Counter elapsed value ≧ Comparison output set value → Comparison output: on



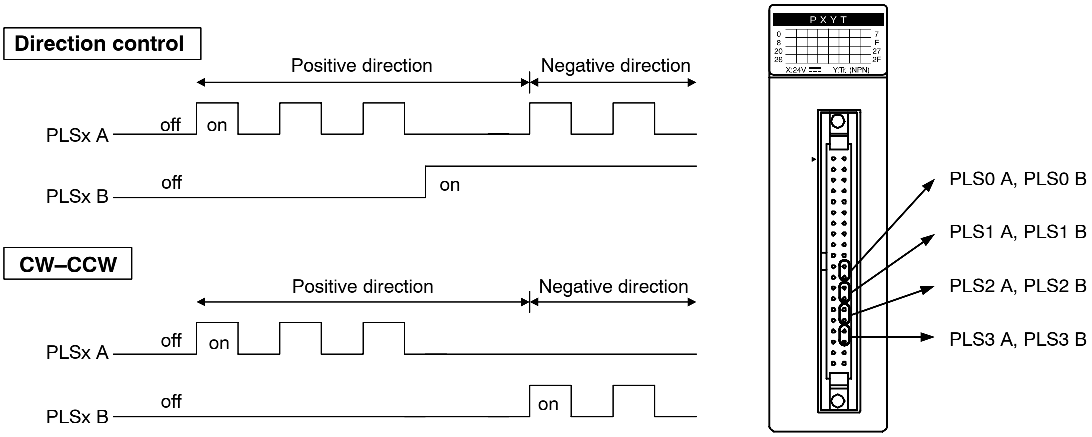
* The on/off of the comparison output can also be specified to correspond to reversed operations. EQx is a signal used for internal processing, and is not output to an external device.

1.2.6 Pulse Output Function

The FP2 Pulse I/O Unit is equipped with four pulse output channels.

The maximum pulse output is 100 kHz, and two modes are available, as described below, for the output format. The output frequency can be specified in units of 1 Hz.

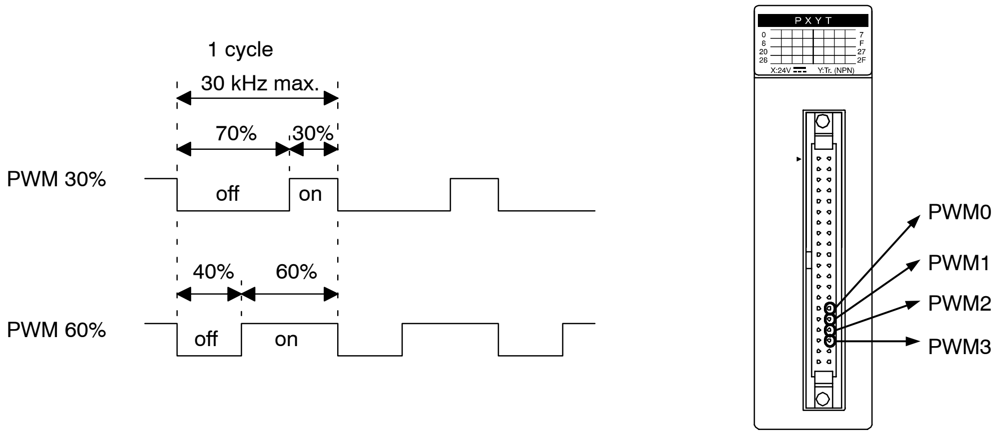
The pulse output can be set so it is input to a high−speed counter through an internal connection to the unit, enabling high−speed processing.



1.2.7 PWM Output Function

The FP2 Pulse I/O Unit is equipped with four PWM output channels.

The maximum PWM output is 30 kHz, and the duty can be specified in units of 1%.



Note

The pulse output function and PWM output function are available only in the FP2 Pulse I/O Unit.

1.3 Restrictions on Unit Combinations

1.3.1 Restrictions on Combinations Based on the Current Consumption

The internal current consumption (at 5 V power supply) of the FP2 High−speed Counter Unit and FP2 Pulse I/O Unit are as shown below. When configuring the system, the usage conditions of other units should be taken into consideration and the overall consumption kept within the allowable range of the power supply unit.

Name	Parts No.	Current consumption (at 5 V power supply)
FP2 High−speed Counter Unit (NPN output)	FP2−HSCT	450 mA or less
FP2 High−speed Counter Unit (PNP output)	FP2−HSCP	450 mA or less
FP2 Pulse I/O Unit (NPN output)	FP2−PXYT	500 mA or less
FP2 Pulse I/O Unit (PNP output)	FP2−PXYP	500 mA or less

◆ **REFERENCE**

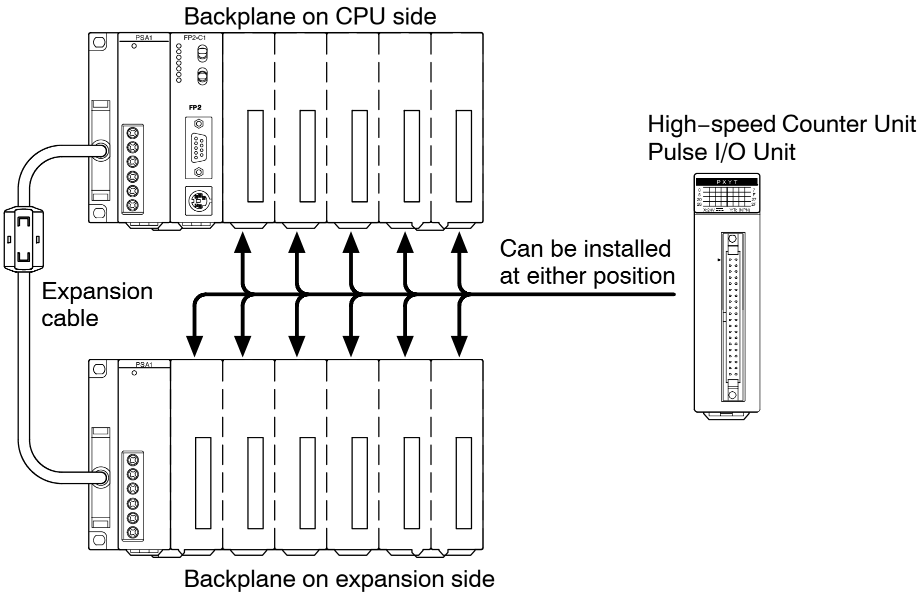
For the internal current consumptions of other units, refer to the “FP2/FP2SH Hardware Manual” and the instruction manual for the pertinent unit.

1.3.2 Restrictions When Using the Unit in Combination with a CPU Unit

The FP2 CPU unit used should be Ver. 1.09 or a subsequent version.

1.3.3 Restrictions on the Unit Installation Position

The FP2 High−speed Counter Unit and FP2 Pulse I/O Unit may be installed on either the backplane on the CPU side, or the backplane on the expansion side. Multiple units may be installed as long as the overall current consumption is within the range described above. However, these units should be installed to the right of the power supply unit and the CPU unit.



1.3.4 Number of Interrupts

If using the unit as a counter unit, there are no restrictions on functions imposed by the number of units, but if using it as an interrupt unit, only two units can be used as interrupt units, with eight interrupts per unit. Please be aware that any other units will have only one interrupt (mode C).

“Unit with Interrupt function” and “Intelligent unit that generate interrupts”

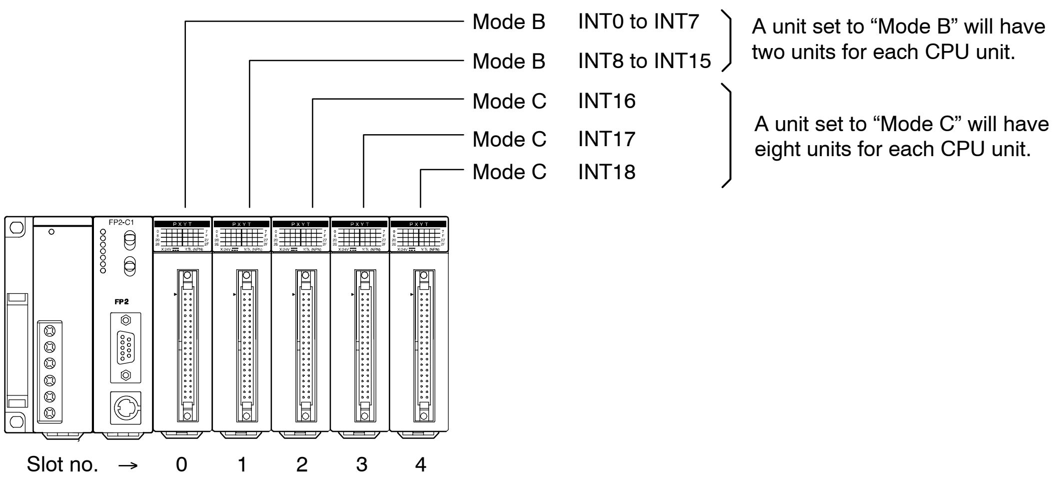
“Unit with Interrupt function”

- When “Mode B” has been specified for the FP2 High−speed Counter Unit and FP2 Pulse I/O Unit, the unit will be treated as an interrupt unit, and eight interrupts per unit will be available for use.
- When “Mode B” has been set for the unit, however, please be aware that only two units can be used with each CPU unit.

“Intelligent unit that generate interrupts”

- When “Mode C” has been specified for the FP2 High−speed Counter Unit and FP2 Pulse I/O Unit, the unit will be treated as an intelligent unit that generates interrupts, and one interrupt per unit will be available for use.
- With an intelligent unit that generates interrupts, however, please be aware that only eight units can be used with each CPU unit.

Interrupt function when multiple units are being used



☞ **Note**

The modes of a unit installed in the FP2 can be used in any combination, but when both “Mode B” and “Mode C” are used in conjunction, be aware that the maximum number of interrupts will be INT23.

1.4 Restrictions Based on Combinations of Functions

With the FP2 Pulse I/O Unit, both pulse output and PWM output are output from the same channels, and up to four channels can be used. If both pulse output and PWM output are being used in combination, however, the pulse output (PLS) should be allocated before the PWM output (PWM), as shown in the table below.

Combination	Channel used			
	CH0	CH1	CH2	CH3
1	PWM	PWM	PWM	PWM
2	PLS	PWM	PWM	PWM
3	PLS	PLS	PWM	PWM
4	PLS	PLS	PLS	PWM
5	PLS	PLS	PLS	PLS

1.5 Restrictions on Setting Values

The values set for the “PLS/PWM Frequency Setting” and the “PWM Duty Setting” of the FP2 Pulse I/O Unit should be within the range of specified values.
Be aware that setting a value which exceeds the specified value can cause malfunction.

Setting		PLS/PWM frequency setting		PWM duty setting	Output pulse
		When using PLS function	When using PWM function		
Specified value		0 Hz *1 to 100.000k Hz	0 Hz *1 to 30.000k Hz	0% to 100%	Normal output
Other than specified value	**Until error is detected**	100.001k Hz to 131.071k Hz	30.001k Hz to 31.457k Hz	—	Normal output *2
	Error detection range	131.072k Hz to 1048.575 k Hz	31.458k Hz to 41.943k Hz	101% to 127%	OFF
	After error is detected	1048.576 k Hz or more	41.944k Hz or more	128% or more	Normal operation does not take place

*1: If 0 Hz is set, no pulses are output.
*2: This is affected by the load conditions, and should not be used.

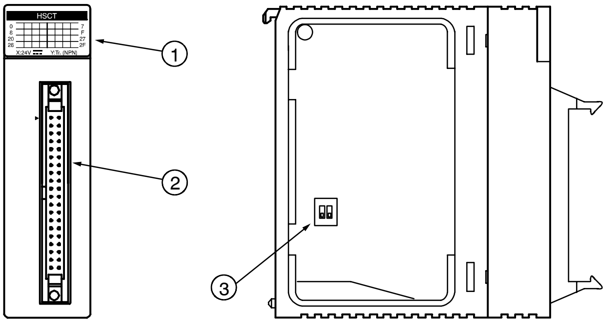
Chapter 2

Part Names and Functions

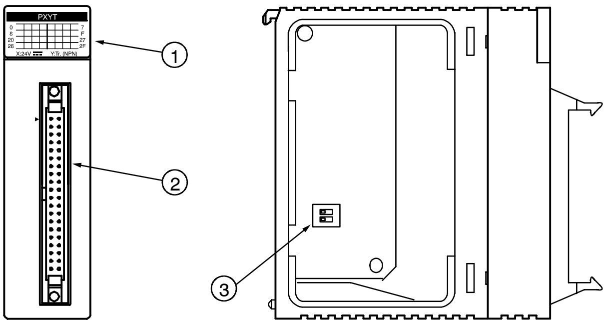
2.1 Part Names and Functions

2.1.1 Part Names and Functions

FP2 High−speed Counter Unit



FP2 Pulse I/O Unit



① **Operation status LEDs**
This lights to reflect the input/output status of the terminal unit. For detailed information, see page 2 – 6.

② **Input/output connector**
This connects the signals input to and output from the unit. For the terminal wiring diagram, see page 3 – 5.

③ **Mode setting switch**
This specifies the interrupt operation mode for the unit. The modes listed below can be specified.
– No interruption
– With Interruption (interrupt points: 8)
– Intelligent unit that generates interrupts (interrupt points: 1)
For detailed information, see page 7 – 3.

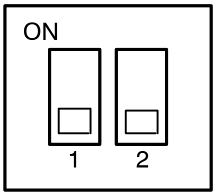
Tip

The settings of the mode setting switches become effective when the power supply is turned on.

2.1.2 Mode Setting Switches

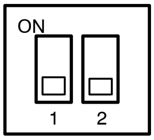
The mode setting switches on the side panel of the unit are used to set the various interrupt functions.

Mode settings switches



SW1	SW2	Mode	Description
off	off	Mode A	No interruption
on	off	Mode B	With Interruption (INT0 to INT7)
off	on	Mode C	Intelligent unit that generates interrupts (only INT0)
on	on	Mode D	Reserved

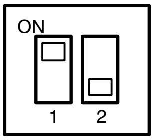
Mode A (SW1 → off, SW2 → off)



No interruption

When this setting is used, the interrupt function will not operate even if used.

Mode B (SW1 → on, SW2 → off)

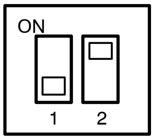


With Interruption (interrupt points: 8)

Up to eight interrupts can be used for each unit (INT0 to INT7).

When this mode is specified, eight interrupt points (INT0 to INT7) are automatically defined for the unit, regardless of whether or not the interrupt function is used.

Mode C (SW1 → off, SW2 → on)



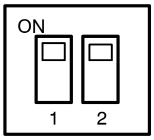
Intelligent unit that generates interrupts (interrupt points: 1)

One interrupt for each unit becomes effective (INT0 *1).

INT1 to INT7 are invalid, even if interrupt settings have been defined for them.

*1: This INT0 defines the interrupt position for the unit. Interrupt program numbers that can be specified in the sequence program are INT16 to 23.

Mode D (SW1 → on, SW2 → on)



Reserved

This setting should not be specified by the user.

Tip

“Unit with interrupt function” and “Intelligent unit that generate interrupt function”

“Unit with interrupt function”

– If “Mode B” has been specified for the FP2 High−speed Counter Unit and FP2 Pulse I/O Unit, the unit will be treated as an interrupt unit, and eight interrupts per unit will be available for use.

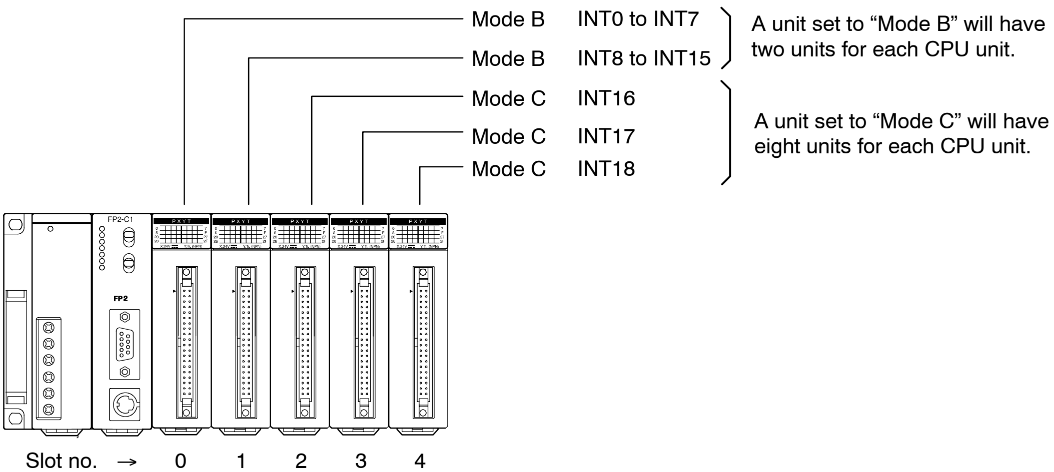
– If “Mode B” has been set for the unit, however, please be aware that only two units can be used with each CPU unit.

“Intelligent unit that generate interrupts”

– If “Mode C” has been specified for the FP2 High−speed Counter Unit and FP2 Pulse I/O Unit, the unit will be treated as an intelligent unit that generates interrupts, and one interrupt per unit will be available for use.

– With an intelligent unit that generates interrupts, however, please be aware that only eight units can be used with each CPU unit.

Interrupt function when multiple units are being used



The modes of a unit installed in the FP2 can be used in any combination, but when both “Mode B” and “Mode C” are used in conjunction, please be aware that the maximum number of interrupts will be INT23.

2.1.3 Operating Status LEDs

The unit LEDs light to reflect the input/output status of the terminal block (input/output connector). Please refer to the allocation tables below.

0	A1	A2	A3	A4	A5	A6	A7	A8	7
8	B1	B2	B3	B4	B5	B6	B7	B8	F
20	A11	A12	A13	A14	A15	A16	A17	A18	27
28	B11	B12	B13	B14	B15	B16	B17	B18	2F

FP2 High−speed Counter Unit allocation table

LED	Function						LED	Function					
	Input	Interrupt	Counter	Compare	Pulse	PWM		Output	Interrupt	Counter	Compare	Pulse	PWM
A1	X0	—	CH0 IN−A	—	—	—	**A11**	Y20	—	—	[CMP0]	—	—
A2	X1	—	CH0 IN−B	—	—	—	**A12**	Y21	—	—	[CMP1]	—	—
A3	X2	—	CH0 Reset	—	—	—	**A13**	Y22	—	—	[CMP2]	—	—
A4	X3	—	CH0 Mask	—	—	—	**A14**	Y23	—	—	[CMP3]	—	—
A5	X4	—	CH1 IN−A	—	—	—	**A15**	Y24	—	—	[CMP4]	—	—
A6	X5	—	CH1 IN−B	—	—	—	**A16**	Y25	—	—	[CMP5]	—	—
A7	X6	—	CH1 Reset	—	—	—	**A17**	Y26	—	—	[CMP6]	—	—
A8	X7	—	CH1 Mask	—	—	—	**A18**	Y27	—	—	[CMP7]	—	—
B1	X8	INT0	CH2 IN−A	—	—	—	**B11**	Y28	—	—	—	—	—
B2	X9	INT1	CH2 IN−B	—	—	—	**B12**	Y29	—	—	—	—	—
B3	XA	INT2	CH2 Reset	—	—	—	**B13**	Y2A	—	—	—	—	—
B4	XB	INT3	CH2 Mask	—	—	—	**B14**	Y2B	—	—	—	—	—
B5	XC	INT4	CH3 IN−A	—	—	—	**B15**	Y2C	—	—	—	—	—
B6	XD	INT5	CH3 IN−B	—	—	—	**B16**	Y2D	—	—	—	—	—
B7	XE	INT6	CH3 Reset	—	—	—	**B17**	Y2E	—	—	—	—	—
B8	XF	INT7	CH3 Mask	—	—	—	**B18**	Y2F	—	—	—	—	—

FP2 Pulse I/O Unit allocation table

LED	Function						LED	Function					
	Input	Interrupt	Counter	Compare	Pulse	PWM		Output	Interrupt	Counter	Compare	Pulse	PWM
A1	X0	—	CH0 IN–A	—	—	—	A11	Y20	—	—	[CMP0]	PLS0 Direction	—
A2	X1	—	CH0 IN–B	—	—	—	A12	Y21	—	—	[CMP1]	PLS1 Direction	—
A3	X2	—	CH0 Reset	—	—	—	A13	Y22	—	—	[CMP2]	PLS2 Direction	—
A4	X3	—	CH0 Mask	—	—	—	A14	Y23	—	—	[CMP3]	PLS3 Direction	—
A5	X4	—	CH1 IN–A	—	—	—	A15	Y24	—	—	[CMP4]	—	—
A6	X5	—	CH1 IN–B	—	—	—	A16	Y25	—	—	[CMP5]	—	—
A7	X6	—	CH1 Reset	—	—	—	A17	Y26	—	—	[CMP6]	—	—
A8	X7	—	CH1 Mask	—	—	—	A18	Y27	—	—	[CMP7]	—	—
B1	X8	INT0	CH2 IN–A	—	—	—	B11	Y28	—	—	—	[PLS0 A]	—
B2	X9	INT1	CH2 IN–B	—	—	—	B12	Y29	—	—	—	[PLS0 B]	—
B3	XA	INT2	CH2 Reset	—	—	—	B13	Y2A	—	—	—	[PLS1 A]	—
B4	XB	INT3	CH2 Mask	—	—	—	B14	Y2B	—	—	—	[PLS1 B]	—
B5	XC	INT4	CH3 IN–A	—	—	—	B15	Y2C	—	—	—	[PLS2 A]	[PWM0]
B6	XD	INT5	CH3 IN–B	—	—	—	B16	Y2D	—	—	—	[PLS2 B]	[PWM1]
B7	XE	INT6	CH3 Reset	—	—	—	B17	Y2E	—	—	—	[PLS3 A]	[PWM2]
B8	XF	INT7	CH3 Mask	—	—	—	B18	Y2F	—	—	—	[PLS3 B]	[PWM3]

[ ]: This is a signal output directly to the I/O connector, and has no relation to the output (Y). However, the status of these signals can be monitored using the input (X) of the same name.

☞ Notes

- **The LED display may waver when a high–speed I/O signal is present, but this does not adversely affect the function.**
- **The table as above shows when the unit is installed into slot 0. I/O number vary according to the slot equipped.**

2.1 Part Names and Functions

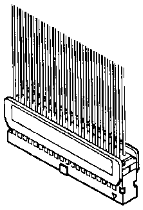
Chapter 3

Wiring

3.1 Connections Using Wire−pressed Terminal Type Connector

3.1.1 Wire−Pressed Terminal Type Connector Specifications

The wire pressed terminal type connector is one that can be connected without stripping the sheath from the wire. Special tools are used for wiring this type of connector.



Wire−pressed terminal type connector (40−pin)

Suitable wires (twisted wire)

Size	Conductor cross-sectional area	Insulation thickness	Rated current
AWG#22	0.3 mm^2	dia. 1.5 to dia. 1.1	3A
AWG#24	0.2 mm^2		

Special tool

Name	Product No.
Pressure connection tool	AXY52000FP

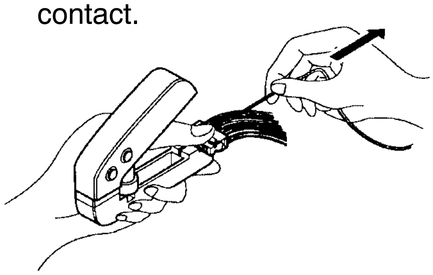
Wire−pressed terminal type connector (provided as accessory with unit)

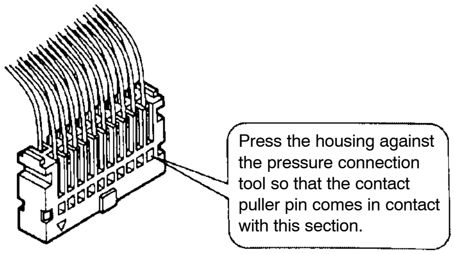
Name	Description	Product No.
Wire−pressed terminal type connector set	two pieces (40−pin, with semi−cover, AWG22, 24)	AFP2801

Tip

Contact Puller Pin for Rewiring

If there is a wiring mistake or the cable is incorrectly pressure-connected, the contact puller pin provided with the fitting can be used to remove the contact.



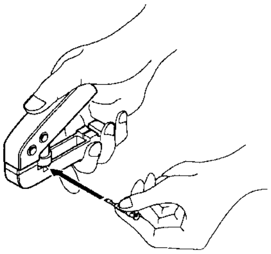


3.1.2 How the Wire−Pressed Type Connector is Used

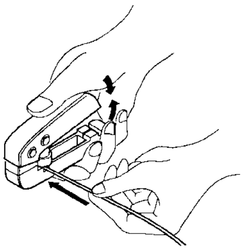
The wire end can be directly crimped without removing the wire's insulation, saving labor.

Procedure:

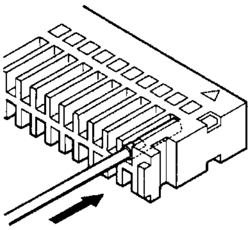
1. **Bend the welder (contact) back from the carrier, and set it in the pressure connection tool.**



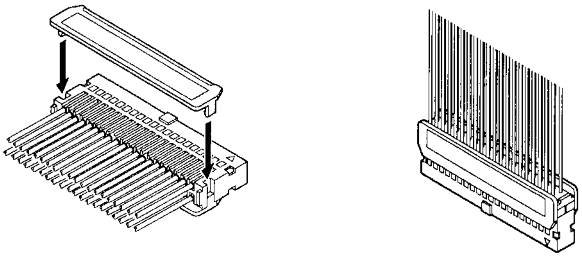
2. **Insert the wire without removing its insulation until it stops, and lightly grip the tool.**



3. **After press-fitting the wire, insert it into the housing.**

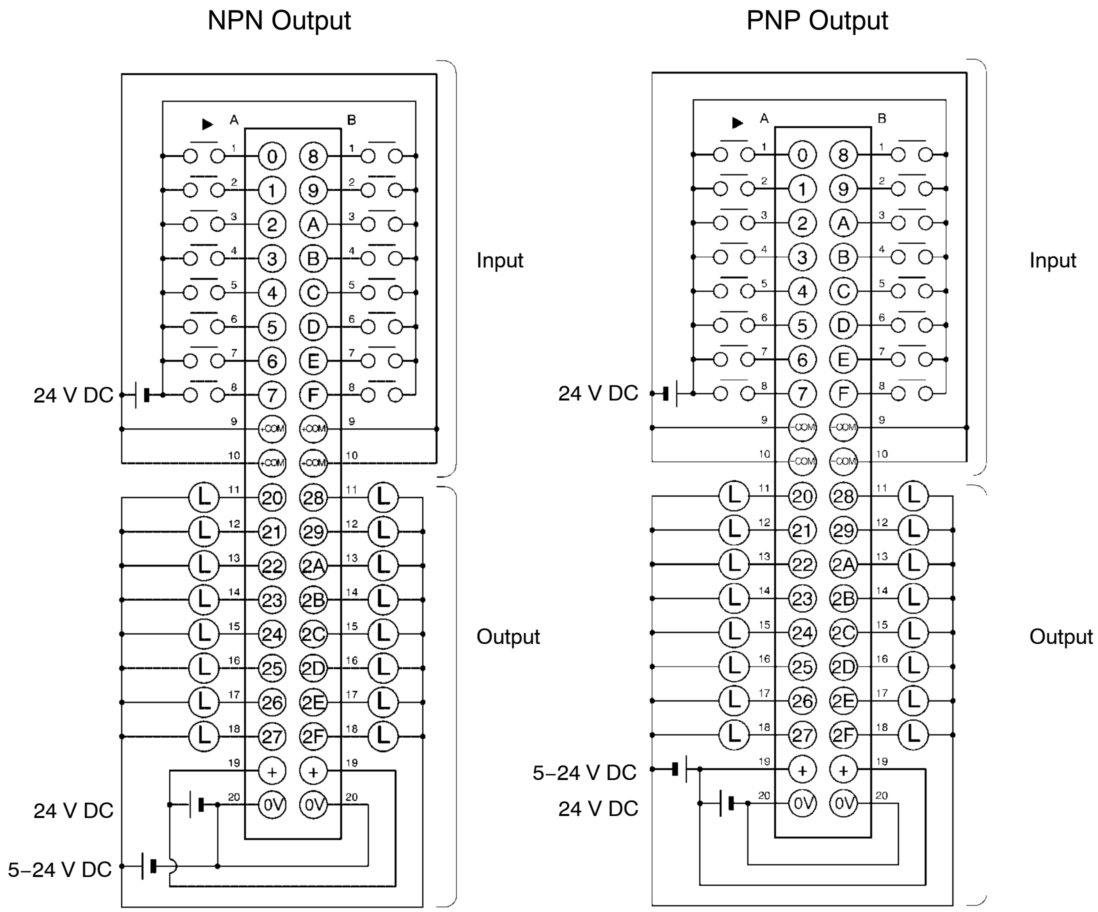


4. **When all wires has been inserted, fit the semi-cover into place.**



3.2 Input/Output Specifications and Connector Pin Wiring Diagram

3.2.1 Terminal Layout Diagram

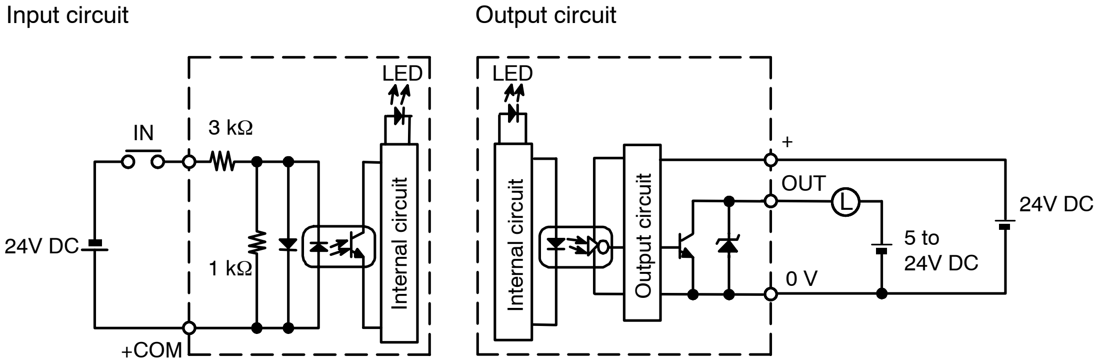


Notes

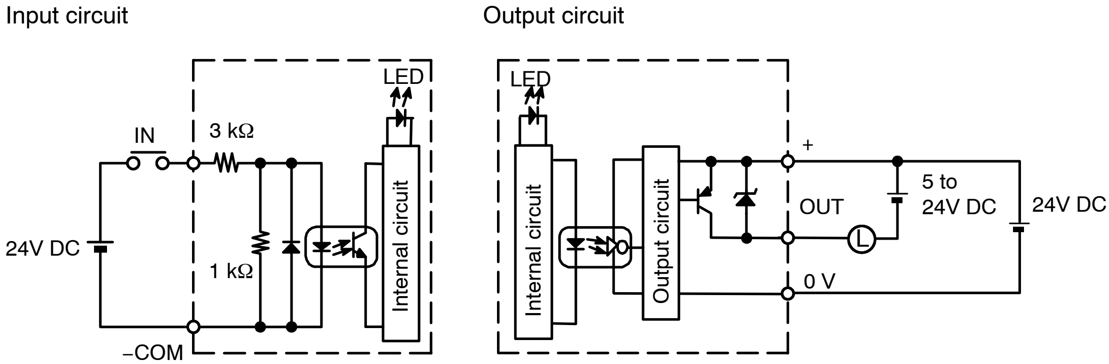
- **The same terminal layout is used in both the FP2 High−speed Counter Unit and the FP2 Pulse I/O Unit.**
- **The COM (4 points), + (2 points) and 0V (2 points) terminals are connected internally.**

3.2.2 Internal Circuit Diagram

NPN output



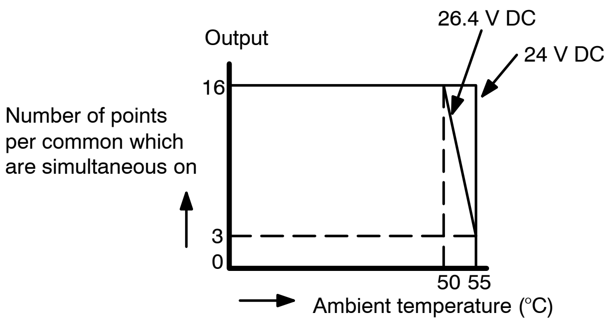
PNP output



The same internal circuit is used in both the FP2 High–speed Counter Unit and the FP2 Pulse I/O Unit.

Note

The number of points that go on simultaneously when there is PNP output should be reduced as shown in the illustration below.



Chapter 4

Units Settings and Confirmation of Design Contents

4.1 Confirming Slot Number and I/O Number Allocations

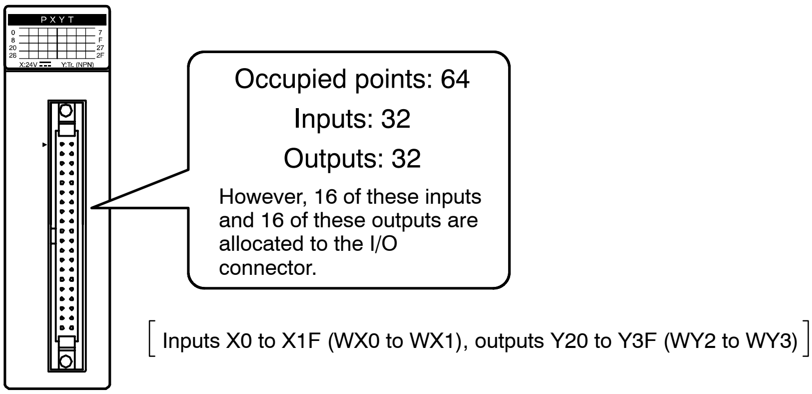
4.1.1 Dedicated I/O Area

In the FP2 High−speed Counter Unit and FP2 Pulse I/O Unit, like other I/O units, inputs (X) and outputs (Y) are allocated in order for the units to be used.

The I/O occupied points of FP2 High−speed Counter Unit and FP2 Pulse I/O Unit are 32 inputs (X0 to X1F)/32 outputs (Y20 to Y3F).

The configuration of the occupied I/O area is as shown below.

Example: When the FP2 High−speed Counter Unit or FP2 Pulse I/O Unit is installed in slot 0



4.1.2 FP2 High−speed Counter Unit I/O Allocation Table

Input Allocation

	External terminal	Function					
		Input	Interrupt	Counter	Comparator	Pulse	PWM
External terminal	A1	X0	—	CH0 IN−A	—	—	—
	A2	X1	—	CH0 IN−B	—	—	—
	A3	X2	—	CH0 Reset	—	—	—
	A4	X3	—	CH0 Mask	—	—	—
	A5	X4	—	CH1 IN−A	—	—	—
	A6	X5	—	CH1 IN−B	—	—	—
	A7	X6	—	CH1 Reset	—	—	—
	A8	X7	—	CH1 Mask	—	—	—
	B1	X8	INT0	CH2 IN−A	—	—	—
	B2	X9	INT1	CH2 IN−B	—	—	—
	B3	XA	INT2	CH2 Reset	—	—	—
	B4	XB	INT3	CH2 Mask	—	—	—
	B5	XC	INT4	CH3 IN−A	—	—	—
	B6	XD	INT5	CH3 IN−B	—	—	—
	B7	XE	INT6	CH3 Reset	—	—	—
	B8	XF	INT7	CH3 Mask	—	—	—
I/Os in the unit	—	X10	—	—	CMP0	—	—
	—	X11	—	—	CMP1	—	—
	—	X12	—	—	CMP2	—	—
	—	X13	—	—	CMP3	—	—
	—	X14	—	—	CMP4	—	—
	—	X15	—	—	CMP5	—	—
	—	X16	—	—	CMP6	—	—
	—	X17	—	—	CMP7	—	—
	—	X18	—	—	—	—	—
	—	X19	—	—	—	—	—
	—	X1A	—	—	—	—	—
	—	X1B	—	—	—	—	—
	—	X1C	—	—	—	—	—
	—	X1D	—	—	—	—	—
	—	X1E	—	—	—	—	—
	—	X1F	—	—	—	—	—

—: No input allocations

☞ **Note**

The I/O numbers in the above chart are for when FP2 High−speed Counter Unit is installed in slot 0. The I/O numbers will change depending on the installation slot.

Detailed Explanation of Occupied I/Os

External inputs

– X0 to XF . . . . Input

These operate as inputs. They can also be monitored as inputs when the interrupt function and counter function are being used.

– INT0 to INT7 . . . . Interrupt function

These are used to input interrupt signals. Interrupt signals are generated as a result of input to the I/O connector, and boot the interrupt program in the ladder program. These are effective only if the connection destination functions as an input terminal in the interrupt settings in the shared memory.

– CHx IN−A, CHx IN−B . . Counter function

These are used to input count signals used for counting. The input for IN−A and IN−B serves as the count signal input. There are three input modes: 1) Direction control, 2) Individual input, and 3) Phase input.

– CHx Reset . . . . Counter function

This is input to reset the counter elapsed value. Inputting this signal resets the counter elapsed value to 0.

– CHx mask . . . . Counter function

This is input to temporarily stop the counter. If this input is on, the counter stops temporarily.

Internal inputs

– X10 to X1F . . . . Input

This input is used to monitor the signals of various functions, such as comparison output.

– CMP0 to CMP7 . . . . Comparison output function

The result of comparing the comparison output set value and counter elapsed value in the shared memory can be monitored as X10 to X17.

(Counter elapsed value) < (Comparison output set value)
→ Comparison output: off

(Counter elapsed value) ≧ (Comparison output set value)
→ Comparison output: on

The on/off of the comparison output can also be specified to correspond to reversed operations.

Output Allocation

	External terminal	Function					
		Output	Interrupt	Counter	Comparator	Pulse	PWM
External terminal	A11	Y20	—	—	[CMP0]	—	—
	A12	Y21	—	—	[CMP1]	—	—
	A13	Y22	—	—	[CMP2]	—	—
	A14	Y23	—	—	[CMP3]	—	—
	A15	Y24	—	—	[CMP4]	—	—
	A16	Y25	—	—	[CMP5]	—	—
	A17	Y26	—	—	[CMP6]	—	—
	A18	Y27	—	—	[CMP7]	—	—
	B11	Y28	—	—	—	—	—
	B12	Y29	—	—	—	—	—
	B13	Y2A	—	—	—	—	—
	B14	Y2B	—	—	—	—	—
	B15	Y2C	—	—	—	—	—
	B16	Y2D	—	—	—	—	—
	B17	Y2E	—	—	—	—	—
	B18	Y2F	—	—	—	—	—
I/Os in the unit	—	Y30	—	CH0 Software reset	—	—	—
	—	Y31	—	CH0 Software mask	—	—	—
	—	Y32	—	CH1 Software reset	—	—	—
	—	Y33	—	CH1 Software mask	—	—	—
	—	Y34	—	CH2 Software reset	—	—	—
	—	Y35	—	CH2 Software mask	—	—	—
	—	Y36	—	CH3 Software reset	—	—	—
	—	Y37	—	CH3 Software mask	—	—	—
	—	Y38	—	—	—	—	—
	—	Y39	—	—	—	—	—
	—	Y3A	—	—	—	—	—
	—	Y3B	—	—	—	—	—
	—	Y3C	—	—	—	—	—
	—	Y3D	—	—	—	—	—
	—	Y3E	—	—	—	—	—
	—	Y3F	—	—	—	—	—

—: No output allocations

[ ]: This is a signal output directly to the I/O connector, and has no relation to the output (Y). However, the status of these signals can be monitored using the input (X) of the same name.

Notes

- **The I/O numbers in the chart are for when FP2 High−speed Counter Unit is installed in slot 0. The I/O numbers will change depending on the installation slot.**
- **With the High−speed Counter Unit, there is no I/O allocation for pulse output or PWM output.**

Detailed Explanation of Occupied I/Os

External outputs

– Y20 to Y2F . . . . Output

These operate as outputs. However, if output of the intelligent unit has been allocated, the advanced−function output is output to the I/O connector. If these are not being used as external outputs, they can be used as internal relays.

– CMP0 to CMP7 . . . . Comparison output function

These output the comparison results calculated in the comparison output function. This output is allocated directly to the external output terminals (A11 to A18), and outputs (Y) (Y20 to 27) can be used as internal relays. The comparison output can be monitored using the internal input (X) of the same name.

Internal outputs

– Y30 to Y3F . . . . Output

These outputs are signals that control the various functions, such as the counter function. If they have not been allocated to a function, they can be used as internal relays.

– CHx Software Reset . . Counter function

This is output to reset the counter elapsed value. These outputs (Y30, Y32, Y34, Y36) are used to reset the counter elapsed value to 0.

– CHx Software Mask . . . Counter function

This is output to temporarily stop the counter. If these outputs (Y31, Y33, Y35, Y37) are on, the counter stops temporarily.

4.1.3 FP2 Pulse I/O Unit I/O Allocation Table

Input Allocation

	External terminal	Function					
		Input	Interrupt	Counter	Comparator	Pulse	PWM
External terminal	A1	X0	—	CH0 IN−A	—	—	—
	A2	X1	—	CH0 IN−B	—	—	—
	A3	X2	—	CH0 Reset	—	—	—
	A4	X3	—	CH0 Mask	—	—	—
	A5	X4	—	CH1 IN−A	—	—	—
	A6	X5	—	CH1 IN−B	—	—	—
	A7	X6	—	CH1 Reset	—	—	—
	A8	X7	—	CH1 Mask	—	—	—
	B1	X8	INT0	CH2 IN−A	—	—	—
	B2	X9	INT1	CH2 IN−B	—	—	—
	B3	XA	INT2	CH2 Reset	—	—	—
	B4	XB	INT3	CH2 Mask	—	—	—
	B5	XC	INT4	CH3 IN−A	—	—	—
	B6	XD	INT5	CH3 IN−B	—	—	—
	B7	XE	INT6	CH3 Reset	—	—	—
	B8	XF	INT7	CH3 Mask	—	—	—
I/Os in the unit	—	X10	—	—	CMP0	—	—
	—	X11	—	—	CMP1	—	—
	—	X12	—	—	CMP2	—	—
	—	X13	—	—	CMP3	—	—
	—	X14	—	—	CMP4	—	—
	—	X15	—	—	CMP5	—	—
	—	X16	—	—	CMP6	—	—
	—	X17	—	—	CMP7	—	—
	—	X18	—	—	—	PLS0 A	—
	—	X19	—	—	—	PLS0 B	—
	—	X1A	—	—	—	PLS1 A	—
	—	X1B	—	—	—	PLS1 B	—
	—	X1C	—	—	—	PLS2 A	PWM0
	—	X1D	—	—	—	PLS2 B	PWM1
	—	X1E	—	—	—	PLS3 A	PWM2
	—	X1F	—	—	—	PLS3 B	PWM3

—: No input allocations

Note

The I/O numbers in the above chart are for when FP2 Pulse I/O Unit is installed in slot 0. The I/O numbers will change depending on the installation slot.

Detailed Explanation of Occupied I/Os

External inputs

– X0 to XF .... Input

These operate as inputs. They can also be monitored as inputs when the interrupt function and counter function are being used.

– INT0 to INT7 .... Interrupt function

These are used to input interrupt signals. Interrupt signals are generated as a result of input to the I/O connector, and boot the interrupt program in the ladder program. These are effective only if the connection destination functions as an input terminal in the interrupt settings in the shared memory.

– CHx IN−A, CHx IN−B . . Counter function

These are used to input count signals used for counting. The input for IN−A and IN−B serves as the count signal input. There are three input modes: 1) Direction control, 2) Individual input, and 3) Phase input.

– CHx Reset .... Counter function

This is input to reset the counter elapsed value. Inputting this signal resets the counter elapsed value to 0.

– CHx mask .... Counter function

This is input to temporarily stop the counter. If this input is on, the counter stops temporarily.

Internal inputs

– X10 to X1F .... Input

This input is used to monitor the signals of various functions, such as comparison output.

– CMP0 to CMP7 .... Comparison output function

The result of comparing the comparison output set value and counter elapsed value in the shared memory can be monitored as X10 to X17.

(Counter elapsed value) < (Comparison output set value)
→ Comparison output: off

(Counter elapsed value) ≧ (Comparison output set value)
→ Comparison output: on

The on/off of the comparison output can also be specified to correspond to reversed operations.

☛ next page

– PLSx A, PLSx B . . . . . . Pulse output function

Pulse signals generated in the pulse output function can be monitored as X18 to X1F. These inputs reflect the pulse signals being output to the I/O connector as internal input.

– PWMx . . . . PWM output function

PWM signals generated in the PWM output function can be monitored as X1C to X1F. These inputs reflect the PWM signals being output to the I/O connector as internal input.

Output Allocation

	External terminal	Function					
		Output	Interrupt	Counter	Comparator	Pulse	PWM
External terminal	A11	Y20	—	—	CMP0	PLS0 Direction	—
	A12	Y21	—	—	CMP1	PLS1 Direction	—
	A13	Y22	—	—	CMP2	PLS2 Direction	—
	A14	Y23	—	—	CMP3	PLS3 Direction	—
	A15	Y24	—	—	CMP4	—	—
	A16	Y25	—	—	CMP5	—	—
	A17	Y26	—	—	CMP6	—	—
	A18	Y27	—	—	CMP7	—	—
	B11	Y28	—	—	—	[PLS0 A]	—
	B12	Y29	—	—	—	[PLS0 B]	—
	B13	Y2A	—	—	—	[PLS1 A]	—
	B14	Y2B	—	—	—	[PLS1 B]	—
	B15	Y2C	—	—	—	[PLS2 A]	[PWM0]
	B16	Y2D	—	—	—	[PLS2 B]	[PWM1]
	B17	Y2E	—	—	—	[PLS3 A]	[PWM2]
	B18	Y2F	—	—	—	[PLS3 B]	[PWM3]
I/Os in the unit	—	Y30	—	CH0 Software reset	—	—	—
	—	Y31	—	CH0 Software mask	—	—	—
	—	Y32	—	CH1 Software reset	—	—	—
	—	Y33	—	CH1 Software mask	—	—	—
	—	Y34	—	CH2 Software reset	—	—	—
	—	Y35	—	CH2 Software mask	—	—	—
	—	Y36	—	CH3 Software reset	—	—	—
	—	Y37	—	CH3 Software mask	—	—	—
	—	Y38	—	—	—	PLS0 Enable	PWM0 Enable
	—	Y39	—	—	—	PLS1 Enable	PWM1 Enable
	—	Y3A	—	—	—	PLS2 Enable	PWM2 Enable
	—	Y3B	—	—	—	PLS3 Enable	PWM3 Enable
	—	Y3C	—	—	—	PLS0 Start	PWM0 Start
	—	Y3D	—	—	—	PLS1 Start	PWM1 Start
	—	Y3E	—	—	—	PLS2 Start	PWM2 Start
	—	Y3F	—	—	—	PLS3 Start	PWM3 Start

—: No output allocations

[ ]: This is a signal output directly to the I/O connector, and has no relation to the output (Y). However, the status of these signals can be monitored using the input (X) of the same name.

☞ **Note**

The I/O numbers in the above chart are for when FP2 Pulse I/O Unit is installed in slot 0. The I/O numbers will change depending on the installation slot.

Detailed Explanation of Occupied I/Os

External outputs

– Y20 to Y2F . . . . Output

These operate as outputs. However, if output of the intelligent unit has been allocated, the advanced−function output is output to the I/O connector. If these are not being used as external outputs, they can be used as internal relays.

– PLSx direction . . . . Pulse output function

The direction of the pulse output is specified using Y20 to Y23. This output can also be used in conjunction with the comparison result output CMPx of the comparison output function. In this case, the comparison result is output to the I/O connector, but this Y output can be used to specify the pulse direction.

– CMP0 to CMP7 . . . . Comparison output function

These output the comparison results calculated in the comparison output function. This output is allocated directly to the external output terminals (A11 to A18), and outputs (Y) (Y20 to 27) can be used as PLS direction or internal relays. The comparison output can be monitored using the internal input (X) of the same name.

– PLSxA, PLSxB . . . . Pulse output function

These are used to output pulses generated in the pulse output function. The signal consists of two outputs, A and B. This output is allocated directly to the external output terminals (B11 to B18), and outputs (Y) (Y28 to Y2F) can be used as internal relays. The output can be monitored as the internal input (X) of the same name.

– PWMx . . . . PWM output function

This is used to output PWM signals generated in the PWM output function. This output is allocated directly to the external output terminals (B15 to B18), and outputs (Y) (Y2C to Y2F) can be used as internal relays. The output can be monitored as the internal input (X) of the same name.

Internal outputs

– Y30 to Y3F . . . . Output

These outputs are signals that control the various functions, such as the counter function. If they have not been allocated to a function, they can be used as internal relays.

– CHx Software Reset . . Counter function

This is output to reset the counter elapsed value. These outputs (Y30, Y32, Y34, Y36) are used to reset the counter elapsed value to 0.

– CHx Software Mask . . . Counter function

This is output to temporarily stop the counter. If these outputs (Y31, Y33, Y35, Y37) are on, the counter stops temporarily.

– PLSx Enable . . . . Pulse output function

This is the pulse output enable signal. Pulses can be output while this output (Y38 to Y3B) is on.

– PLSx Start . . . . Pulse output function

This is the pulse output start signal (Y3C to Y3F). It is valid only while pulse output is enabled.

– PWMx Enable . . . . PWM output function

This is the PWM output enable signal. PWM can be output while this output (Y38 to Y3B) is on.

– PWMx Start . . . . PWM output function

This is the PWM output start signal (Y3C to Y3F). It is valid only while PWM output is enabled.

4.1.4 Confirming the Allocated I/O Numbers and Slot Numbers

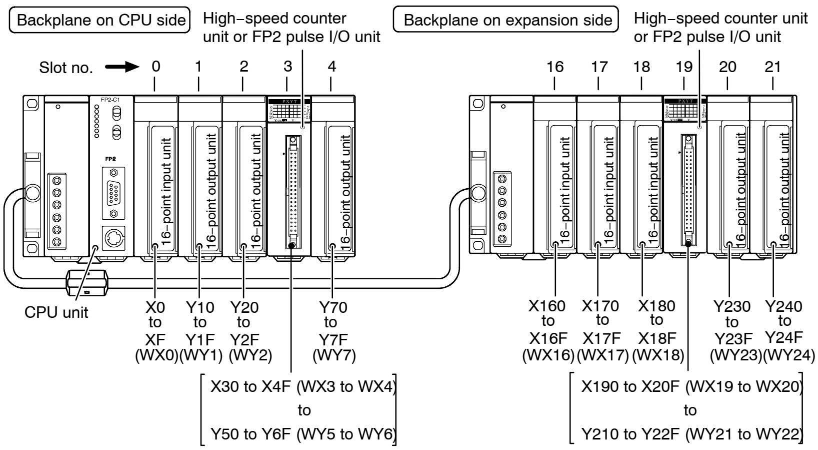
I/O numbers and slot numbers are always necessary in order to create a program. These change depending on the position at which the unit is installed on the backplane. Always check to make sure these have been allocated as indicated in the designs.

Confirming I/O Number Allocations

Check the occupied I/O areas in all of the units that have been installed between the CPU unit and the FP2 High−speed Counter Unit or FP2 Pulse I/O Unit. The area starting from the serial number is allocated as the I/O area of the FP2 High−speed Counter Unit and FP2 Pulse I/O Unit.

Example:

When the FP2 High−speed Counter Unit or FP2 Pulse I/O Unit has been installed in the next slot after the three 16−point units:



Notes

- **When “I/O mount allocation” and “Automatic allocation” have been carried out, 16 points are automatically allocated to empty slots for each of these.**
- **If the CPU unit being used is a dual−module type, also check the I/O area dedicated by the unit incorporated in the CPU unit.**

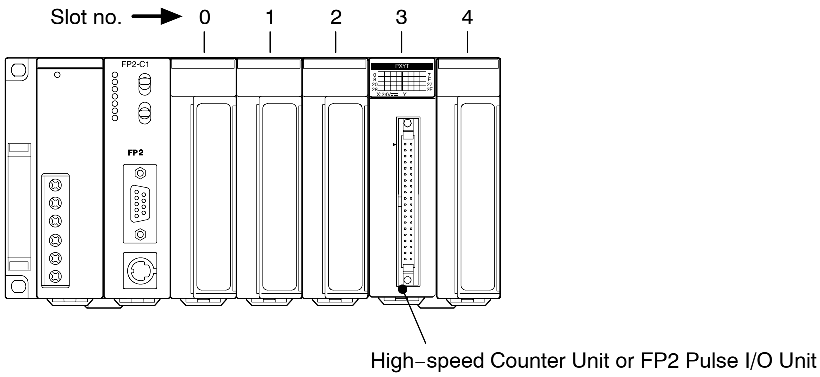
◆ REFERENCE

The slot numbers for the expansion slots start with 16. For information on how other I/O allocations are made, refer to “I/O Allocations” in the “FP2/FP2SH Hardware Manual”.

Confirming Slot Numbers

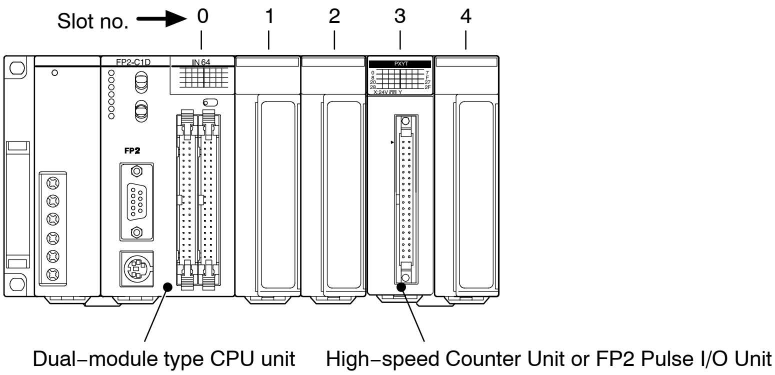
When installed on the CPU backplane

Slots are numbered sequentially, with the slot to the right of the CPU being “0”.

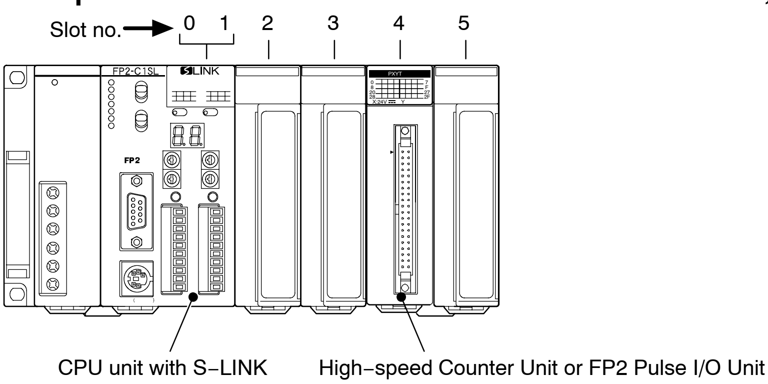


Notes

- **If the CPU unit being used is a dual−module type, the slot of the unit incorporated into the CPU unit should be numbered “0”.**

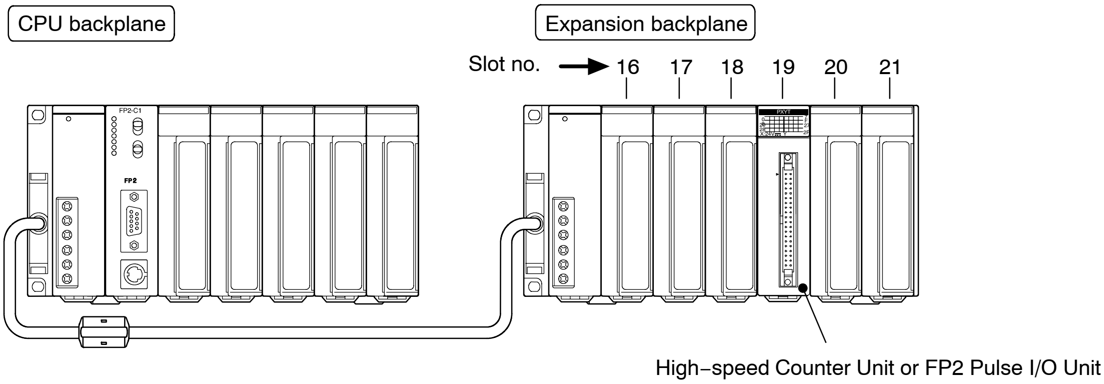


- **If using a CPU unit with an S−LINK, the slots of the unit incorporated into the CPU unit should be numbered “0, 1”.**



When installed on the expansion backplane

The slot to the right of the power supply unit on the expansion backplane should be numbered “16”.



4.2 Internal Counter

4.2.1 How the Internal Counter Works

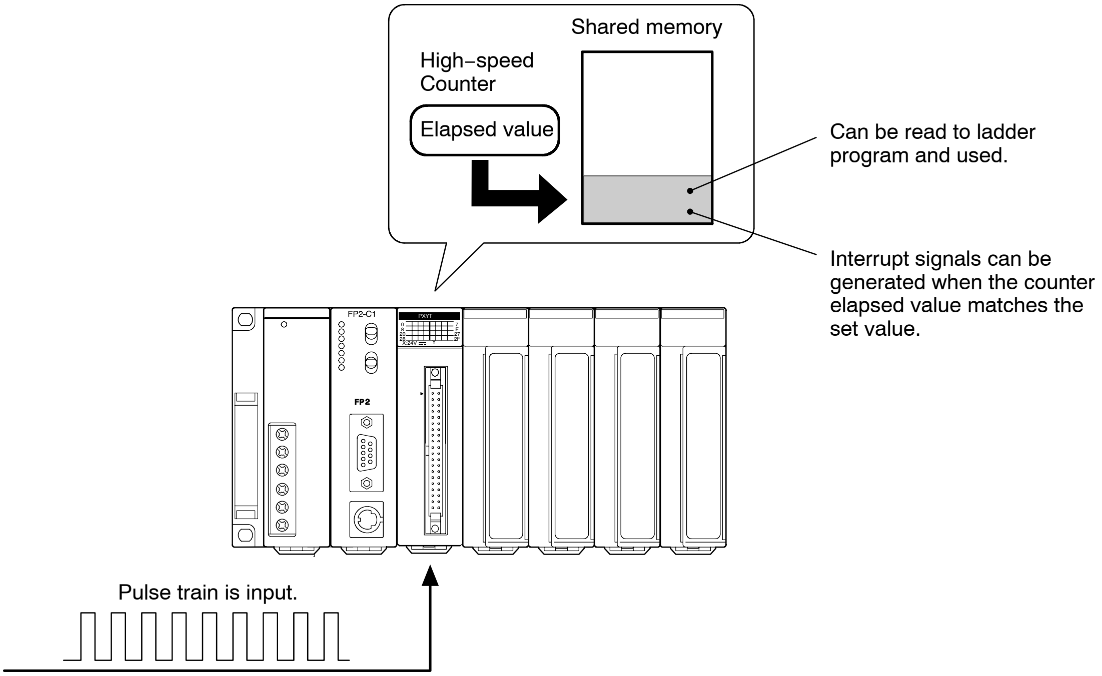
How the Internal Counter Works

The FP2 High−speed Counter Unit/FP2 Pulse I/O Unit has an internal counter that counts the number of pulses input.

The counted values are stored in the shared memory area for each of the channels.

The stored values can be read with a user program to find out the elapsed value.

Using the comparison function, external output can be obtained in response to the counter value.



Operation of the Internal Counter

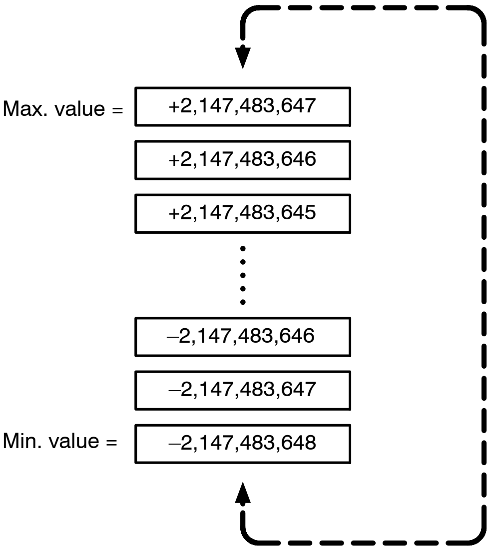
When the power supply is turned off, the counter value is set to 0.

The count value (elapsed value) stored in the shared memory can be read using high−level instructions “F150 (READ)/P150 (PREAD)”.

The count value (elapsed value) can be overwritten using high−level instructions “F151 (WRT)/P151 (PWRT)”.

Calculation Range of the Counter

–2,147,483,648 to +2,147,483,647 (32−bit, with sign)



If the elapsed value exceeds the maximum value (minimum value), it returns to the minimum value (maximum value). No error occurs at that point.

Shared Memory Address in Which the Counter Value is Stored

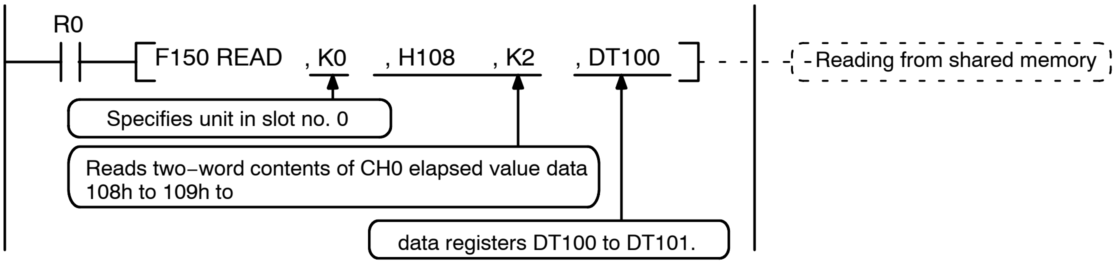
Shared memory address (hexadecimal)		Description	
CH0	**108h, 109h**	Elapsed value count	32−bit, with sign –2,147,483,648 to +2,147,483,647
CH1	**10Ah, 10Bh**		
CH2	**10Ch, 10Dh**		
CH3	**10Eh, 10Fh**		

4.2.2 Reading the Elapsed Value

High−level instructions “F150 (READ)/P150 (PREAD)” are used to read the count value (elapsed value) from the shared memory of the FP2 High−speed Counter Unit and FP2 Pulse I/O Unit.

F150 (READ) and P150 (PREAD) Instructions

These instructions are used to read data from the shared memory of the intelligent unit.



These commands read two words of the CH0 counter elapsed value data stored in the shared memory of the unit installed in slot 0, and store it in DT100 to DT101.

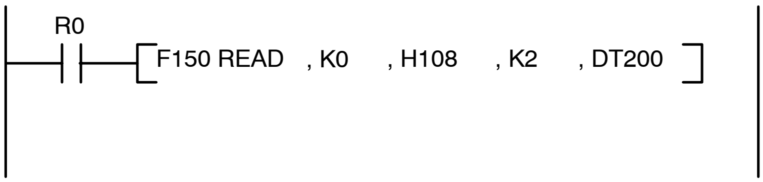
Addresses that are Specified

The data (elapsed value) is stored as 32−bit data.

Shared memory address (hexadecimal)		Description	
CH0	108h, 109h	Elapsed value count	32−bit, with sign −2,147,483,648 to +2,147,483,647
CH1	10Ah, 10Bh		
CH2	10Ch, 10Dh		
CH3	10Eh, 10Fh		

Program Example

This shows the counter elapsed value being read to any desired data register (DT200).

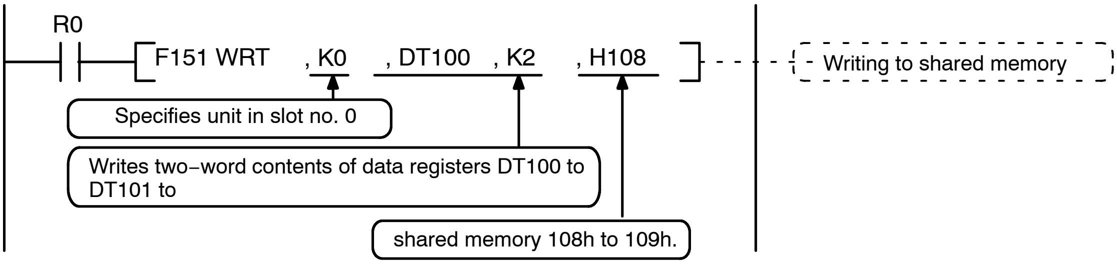


4.2.3 Writing the Elapsed Value

High−level instructions “F151 (WRT)/P151 (PWRT)” are used to write the count value (elapsed value) to the shared memory of the FP2 High−speed Counter Unit and FP2 Pulse I/O Unit.

F151 (WRT) and P151 (PWRT) Instructions

These instructions are used to write data to the shared memory of the intelligent unit.



These commands store the two words of the data in DT100 to DT101 as the CH0 counter elapsed value data stored in the shared memory of the unit installed in slot 0.

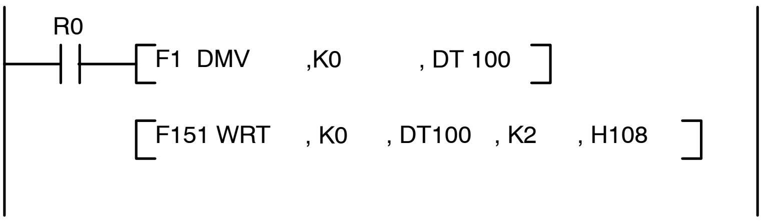
Addresses that are Specified

The data (elapsed value) is stored as 32−bit data.

Shared memory address (hexadecimal)		Contents	
CH0	108h, 109h	Elapsed value count	32−bit, with sign −2,147,483,648 to +2,147,483,647
CH1	10Ah, 10Bh		
CH2	10Ch, 10Dh		
CH3	10Eh, 10Fh		

Program Example

When “0” is written as the counter elapsed value.



Chapter 5

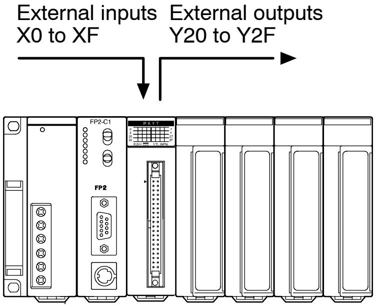
Using the General I/O Function

5.1 About the General I/O Function

5.1.1 What is the General I/O Function?

The general I/O function refers to general input and output as typified by an input unit and an output unit. The FP2 High–speed Counter Unit/FP2 Pulse I/O Unit has advanced functions such as a counter function, but inputs and outputs that have not been allocated to functions operate as general I/O.

When used in conjunction with the input time constant function, the general I/O serves as I/O for the input time constant function, enabling I/O with a high level of noise resistance.



The above I/O numbers are examples that apply when the FP2 High–speed Counter Unit or FP2 Pulse I/O Unit is installed in slot 0.

5.1.2 How I/O are Used as General I/O

With the FP2 High–speed Counter Unit and FP2 Pulse I/O Unit, all I/Os can be used as general I/O. If they have been allocated to a function, however, that allocation takes precedence.

To use the unit as a general I/O, it should be used in its default state. It is not necessary to enter settings for the mode setting switches or the shared memory.

If the FP2 High–speed Counter Unit or FP2 Pulse I/O Unit has been installed in slot 0, inputs X0 to XF and outputs Y20 to Y2F can be used as relays for external input and output.

Tip

Terminals that have not been allocated to functions can be used as general I/O, so that, for example, both counter functions and sensor input can be handled with a single FP2 High–speed Counter Unit or FP2 Pulse I/O Unit. This enables a streamlined, efficient system configuration with no waste.

5.1 About the General I/O Function

Chapter 6

Using the Input Time Constant Function

6.1 About the Input Time Constant Function

6.1.1 What is the Input Time Constant Function?

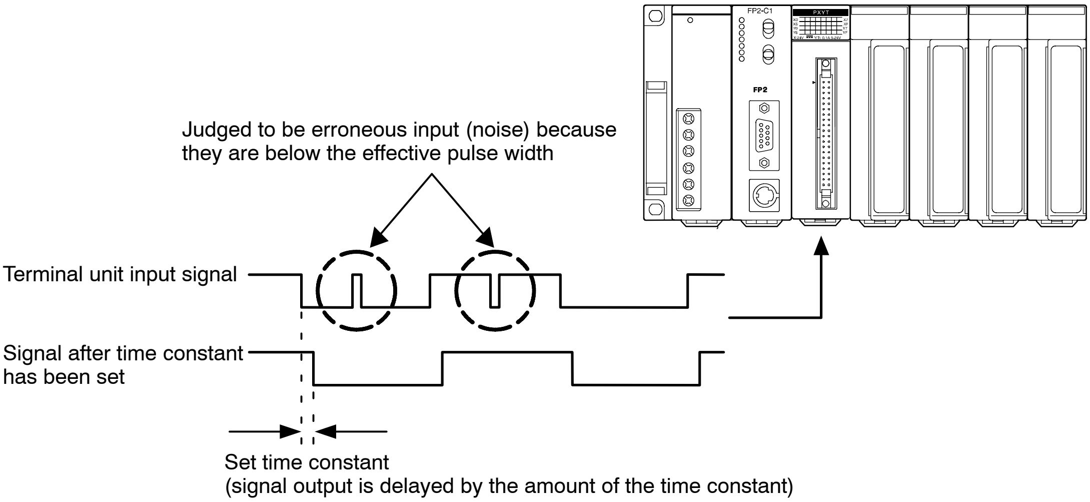
The input time constant function specifies an effective pulse width for input signals from an external input terminal. Any input signals below the effective pulse width are judged to be noise.

The time constant can be selected from among the four values given below. Any width at or above the set value is recognized as a signal.

1) 4 μs
2) 8 μs
3)16 μs
4) 32 μs

Separate time constants can be set for the eight groups of external input terminals listed below.

1) External input terminals A1, A2 (input allocation X0, X1)
2) External input terminals A3, A4 (input allocation X2, X3)
3) External input terminals A5, A6 (input allocation X4, X5)
4) External input terminals A7, A8 (input allocation X6, X7)
5) External input terminals B1, B2 (input allocation X8, X9)
6) External input terminals B3, B4 (input allocation XA, XB)
7) External input terminals B5, B6 (input allocation XC, XD)
8) External input terminals B7, B8 (input allocation XE, XF)



Tip

The input time constant function can be used in conjunction with other functions, such as the interrupt and counter functions.

6.1.2 Setting the Input Time Constant Function

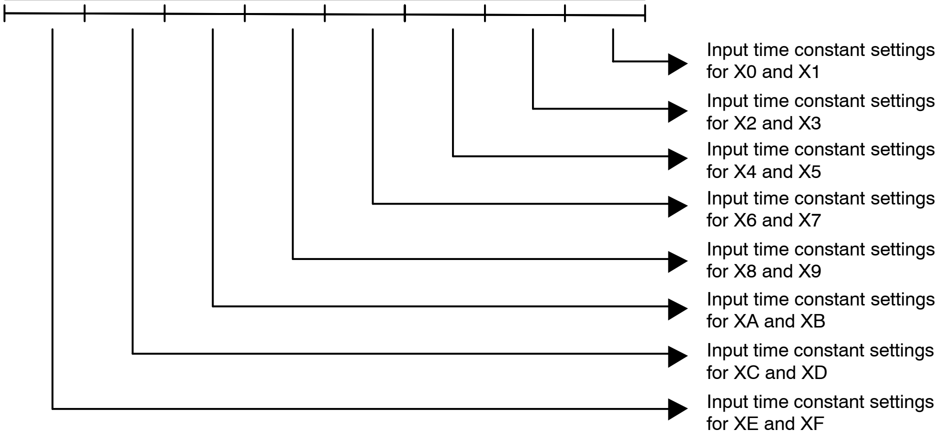
To use the input time constant function, settings must be entered in the shared memory.

Use the shared memory settings to enter input time constant settings for the group of eight external input terminals.

The input time constants are set for the external input terminals, so the settings for the various function allocations corresponding to inputs X0 to XF also become effective (counter input and interrupt input).

Addresses: 13Ch, 13Dh

Input time constant settings	b31 to b28	b27 to b24	b23 to b20	b19 to b16	b15 to b12	b11 to b8	b7 to b4	b3 to b0



Input time constant settings

Set value (HEX)	Function	
	Input time constant	Effective pulse width
0	Used	4 μs
1		8 μs
2		16 μs
3		32 μs
4	Invalid *1	Invalid *1
5		
6		
7		
8		
9		
A		
B		
C		
D		
E		
F	Not used *2	—

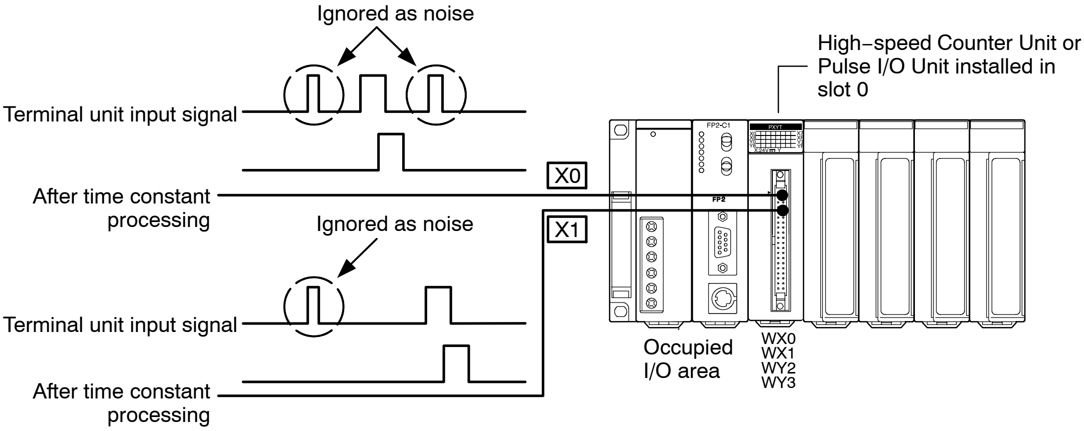
*1: This setting should not be used.
*2: When the power supply is turned on, the default value of “Not used” is set for this.

Note

The shared memory should always be accessed in two–word units.

6.2 Using the Input Time Constant Function

6.2.1 Overview

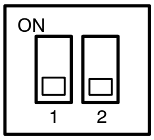


Time constants are set for the X0 and X1 input, and any signals below those widths are ignored as noise.

6.2.2 Setting the Mode Setting Switches

If no interrupts are being used, “Mode A” should be set.

Mode A (SW1 → off, SW2 → off)



No interruption

When this setting is used, the interrupt function will not operate even if used.

The input time constant function can be used regardless of whether the interrupt function is set to “Used” or “Not Used”.

6.2.3 Shared Memory Settings

Setting the time constant.

Sets the input time constant.
In the example, a time constant of 16 μs is set for the inputs X0 and X1, so the value "FFFFFFF2" should be written to addresses 13Ch and 13Dh in the shared memory.

Setting of shared memory addresses 13Ch and 13Dh.

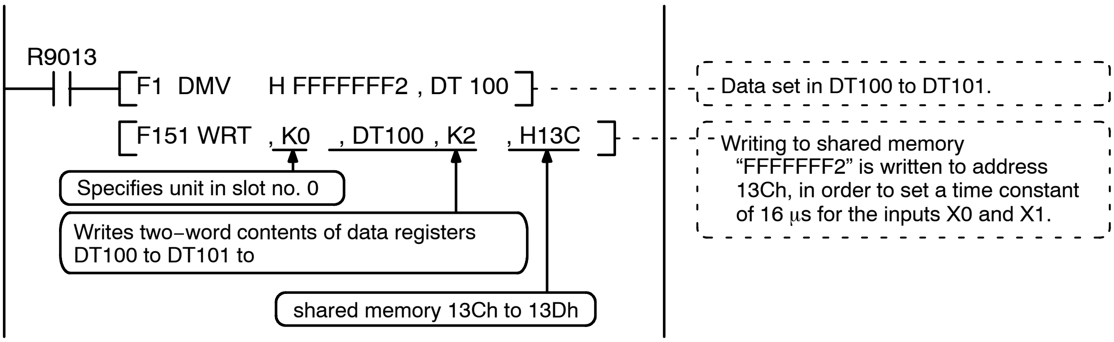
(bit)	32			16	15			0
External input	XF, XE	XD, XC	XB, XA	X9, X8	X7, X6	X5, X4	X3, X2	X1, X0
Set value	F	F	F	F	F	F	F	2
Input time constant setting	Not used	Not used	Not used	Not used	Not used	Not used	Not used	16 μs

◆ **REFERENCE**

For information on shared memory addresses, see page 13 – 12.

6.2.4 Sample Program

This program writes the value "FFFFFFF2" to the time constant setting area (13Ch and 13Dh) of the shared memory addresses, and sets a time constant of 16 μs for the inputs X0 and X1.



6.2 Using the Input Time Constant Function

Chapter 7

Using the Interrupt Function

7.1 About the Interrupt Function

7.1.1 What is the Interrupt Function?

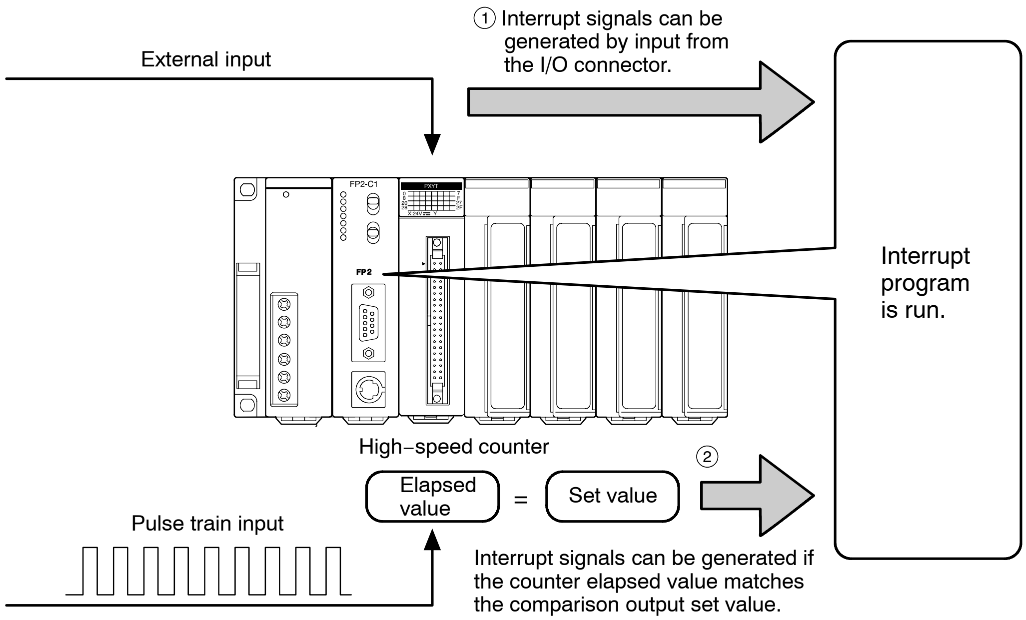
The interrupt function runs an interrupt program that has been created ahead of time, in response to an interrupt signal generated by the unit.

The FP2 High−speed Counter Unit and FP2 Pulse I/O Unit can be used in two ways: as an interrupt unit that has eight interrupts, or as an intelligent unit that generates interrupts, in which case it has only one interrupt.

One feature of the FP2 High−speed Counter Unit and FP2 Pulse I/O Unit are that the connection destination (condition) that generates interrupt signals can be selected.

① Interrupt signals can be generated by input from the I/O connector.

② Interrupt signals can be generated if the counter elapsed value matches the comparison output set value.



Note

Interrupt output based on counter matching is generated when the elapsed value matches the comparison output set value, regardless of whether the count is being incremented or decremented.

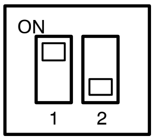
7.1.2 Entering Settings for the Interrupt Function

Two steps are necessary in order to use the interrupt function: setting the mode setting switches, and entering settings in the shared memory. The settings of the mode setting switches become effective when the power supply is turned on.

Procedure 1: Setting the mode setting switches

Follow the procedure described under “Mode setting switches” on page 2 − 4 to set one of the two modes described below.

Mode B (SW1 → on, SW2 → off)

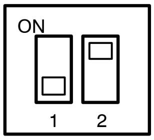


With Interruption (interrupt points: 8)

Up to eight interrupts can be used for each unit (INT0 to INT7).

If this mode is specified, eight interrupt points (INT0 to INT7) are automatically defined for the unit, regardless of whether or not the interrupt function is used.

Mode C (SW1 → off, SW2 → on)



Intelligent unit that generates interrupts (interrupt points: 1)

One interrupt for each unit becomes effective (INT0 *1).

INT1 to INT7 are invalid, even if interrupt settings have been defined for them.

*1: This INT0 defines the interrupt position for the unit. Interrupt program numbers that can be specified in the sequence program are INT16 to 23.

Tip

“Unit with Interrupt function” and “Intelligent unit that generate interrupts”

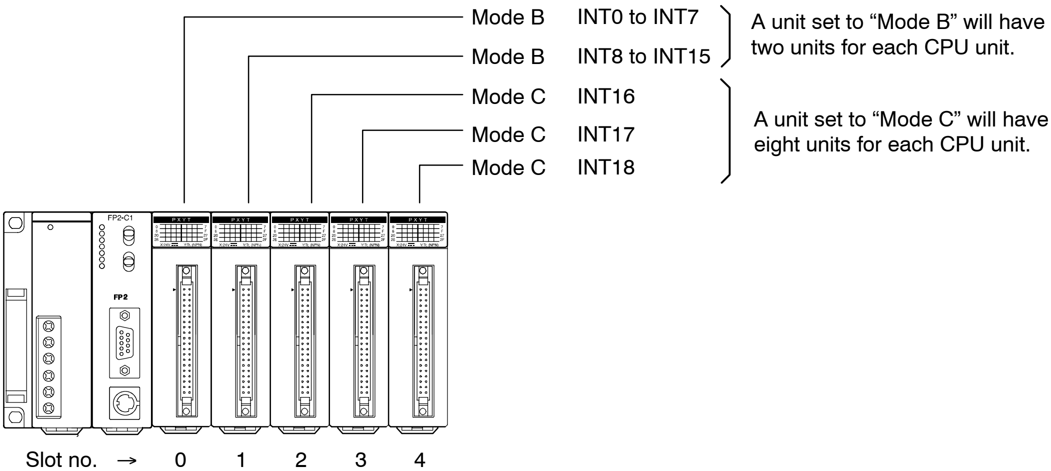
“Unit with Interrupt function”

– When “Mode B” has been specified for the FP2 High−speed Counter Unit and FP2 Pulse I/O Unit, the unit will be treated as an interrupt unit, and eight interrupts per unit will be available for use.
– When “Mode B” has been set for the unit, only two units can be used with each CPU unit.

“Intelligent unit that generate interrupts”

– When “Mode C” has been specified for the FP2 High−speed Counter Unit and FP2 Pulse I/O Unit, the unit will be treated as an intelligent unit that generates interrupts, and one interrupt per unit will be available for use.
– With an intelligent unit that generates interrupts, only eight units can be used with each CPU unit.

Interrupt function when multiple units are being used



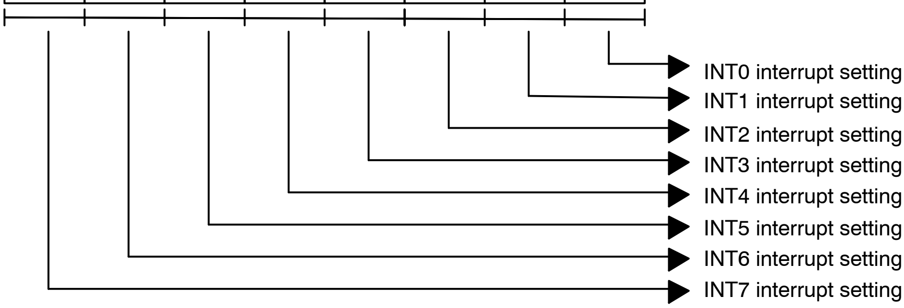
The modes of a unit installed in the FP2 can be used in any combination, but if both “Mode B” and “Mode C” are used in conjunction, please be aware that the maximum number of interrupts will be INT23.

Procedure 2: Entering shared memory settings

After the mode setting switches have been set, settings must be entered in the shared memory. Set the interrupt function mode as indicated in the table below.

Addresses: 138h, 139h

Interrupt setting	b31 to b28	b27 to b24	b23 to b20	b19 to b16	b15 to b12	b11 to b8	b7 to b4	b3 to b0



Set value (HEX)	Function		
	Interrupt function	**Connection destination**	**Interrupt generating conditions**
0	Used	Comparison output function *1 (CMP0 to CMP7)	When output matches
1			
2		Input terminals (X8 to XF)	Off → On
3			On → Off *2
4	Invalid *3	Invalid *3	Invalid *3
5			
6			
7			
8			
9			
A			
B			
C			
D			
E			
F	Not used *4	—	—

*1: INT0 to INT7 correspond to CMP0 to CMP7.
Example: If "Set value 1" is selected for the INT0 interrupt setting, an interrupt is generated if CMP0 matches the output (EQ0).
*2: When this setting has been selected, always execute an interrupt clear command after entering the setting.
*3: No settings should be entered for set values H4 to HE.
*4: When the power supply is turned on, the default value of "Not used" is set for this.

Note

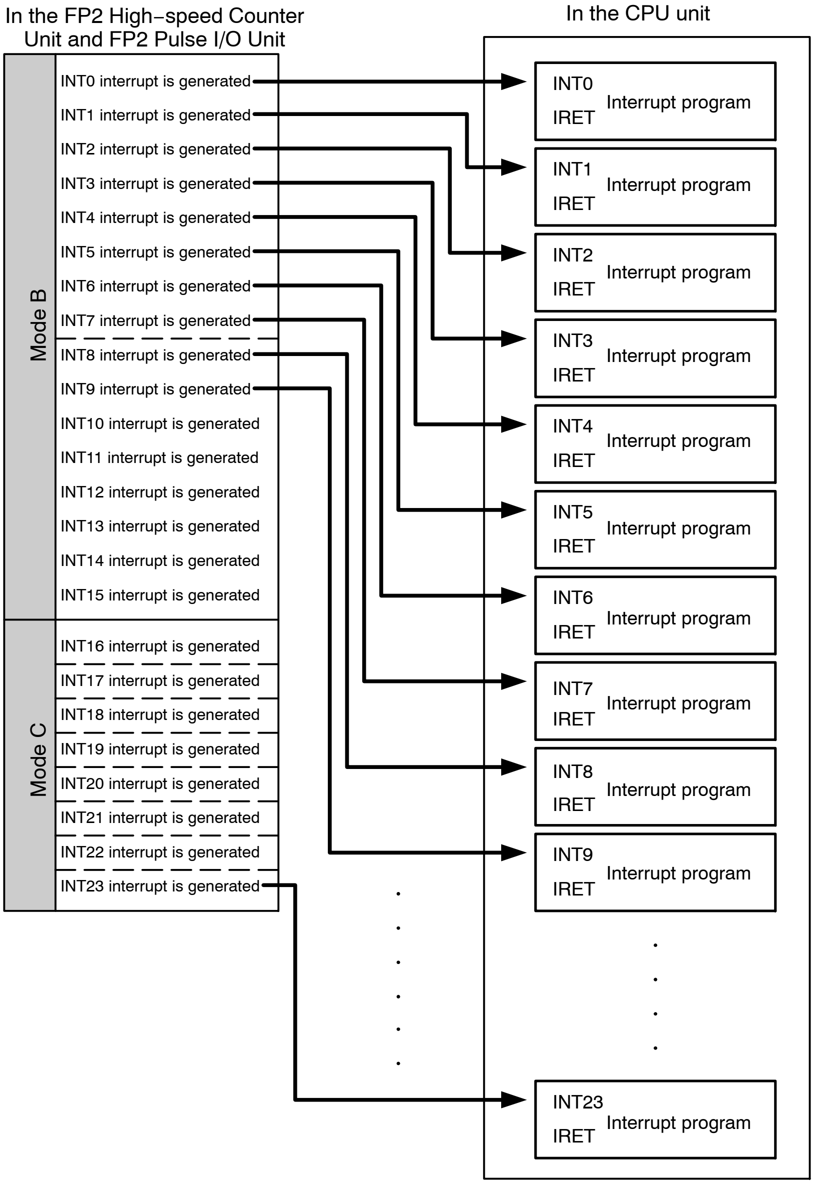
The shared memory should always be accessed in two−word units.

◆ REFERENCE

For information on shared memory addresses, see page 13 – 12.

7.1.3 Relationship Between the Interrupt Input Number and the Interrupt Program

The interrupts of the FP2 High−speed Counter Unit/FP2 Pulse I/O Unit and the interrupt program in the sequence program operate in conjunction.
As shown in the table below, when the INT0 interrupt of the unit has been generated, the interrupt program in the sequence program is executed from INT0 to IRET.



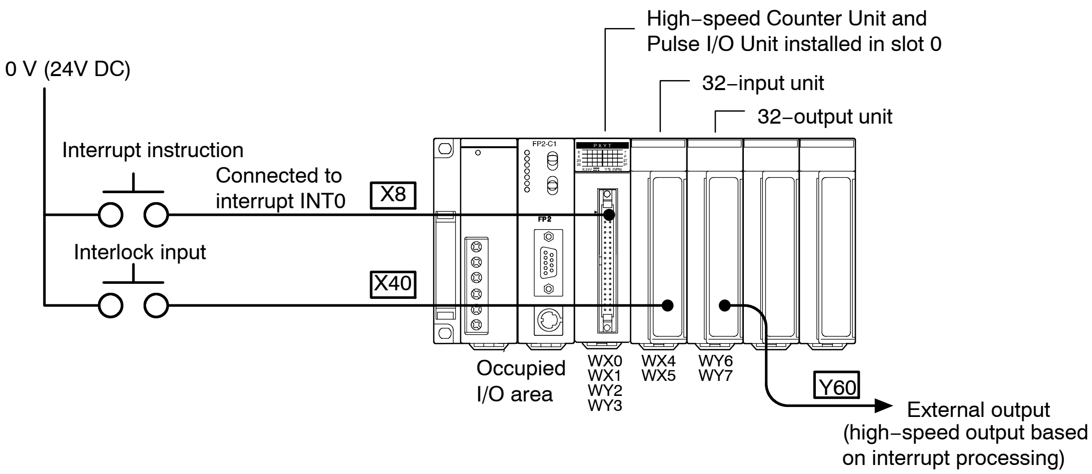
If Mode C has been set, interrupt program numbers that can be specified in the sequence program are INT16 to 23.

◆ **REFERENCE**

For a detailed explanation of the interrupt program, refer to the FP series programming manual.

7.2 Using the Interrupt Function Based on External Input

7.2.1 Overview

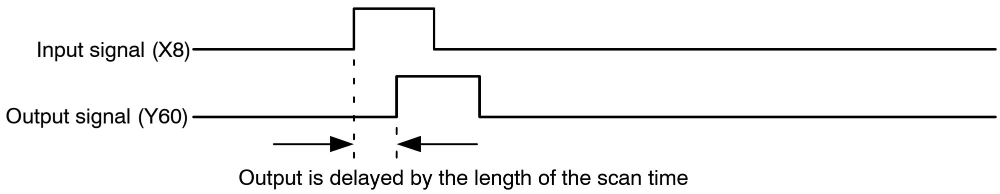


If the X8 interrupt (INT0) is input when the interlock input X40 has been input, the output from Y60 is output at high speed, using interrupt processing.

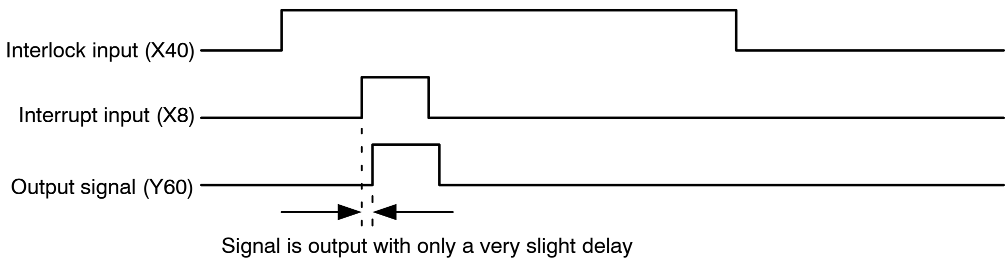
7.2.2 Timing Chart

In normal processing, when interrupt processing is not used, the processing time is affected by the scan time, from when the input is first received to when the signal is output. When interrupt processing is carried out, however, the input state is affected very little by the scan time, so the output only delays slightly.

Normal processing



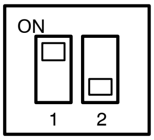
Interrupt processing



7.2.3 Setting the Mode Setting Switches

Set the mode setting switches to Mode B, so that all eight interrupts from INT0 to INT7 can be used. If only one interrupt is needed per unit, the mode can be set to Mode C. When Mode C is used, however, please be aware that the interrupt signal will be INT16.

Mode B (SW1 → on, SW2 → off)

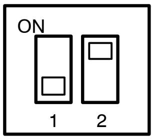


With Interruption (interrupt points: 8)

Up to eight interrupts can be used for each unit (INT0 to INT7).

When this mode is specified, eight interrupt points (INT0 to INT7) are automatically defined for the unit, regardless of whether or not the interrupt function is used.

Mode C (SW1 → off, SW2 → on)



Intelligent unit that generates interrupts (interrupt points: 1)

One interrupt for each unit becomes effective (INT0 *1).

INT1 to INT7 are invalid, even if interrupt settings have been defined for them.

*1: This INT0 defines the interrupt position for the unit. Interrupt program numbers that can be specified in the sequence program are INT16 to 23.

7.2.4 Shared Memory Settings

Interrupt setting

When the interrupt function is being used, settings must be entered in the shared memory, in addition to setting the mode setting switches on the side panel of the main unit.
In the example, an interrupt signal is generated with the rise (off → on) of the external input of X8, so a value of “FFFFFFF2” will be written to addresses 138h and 139h of the shared memory.

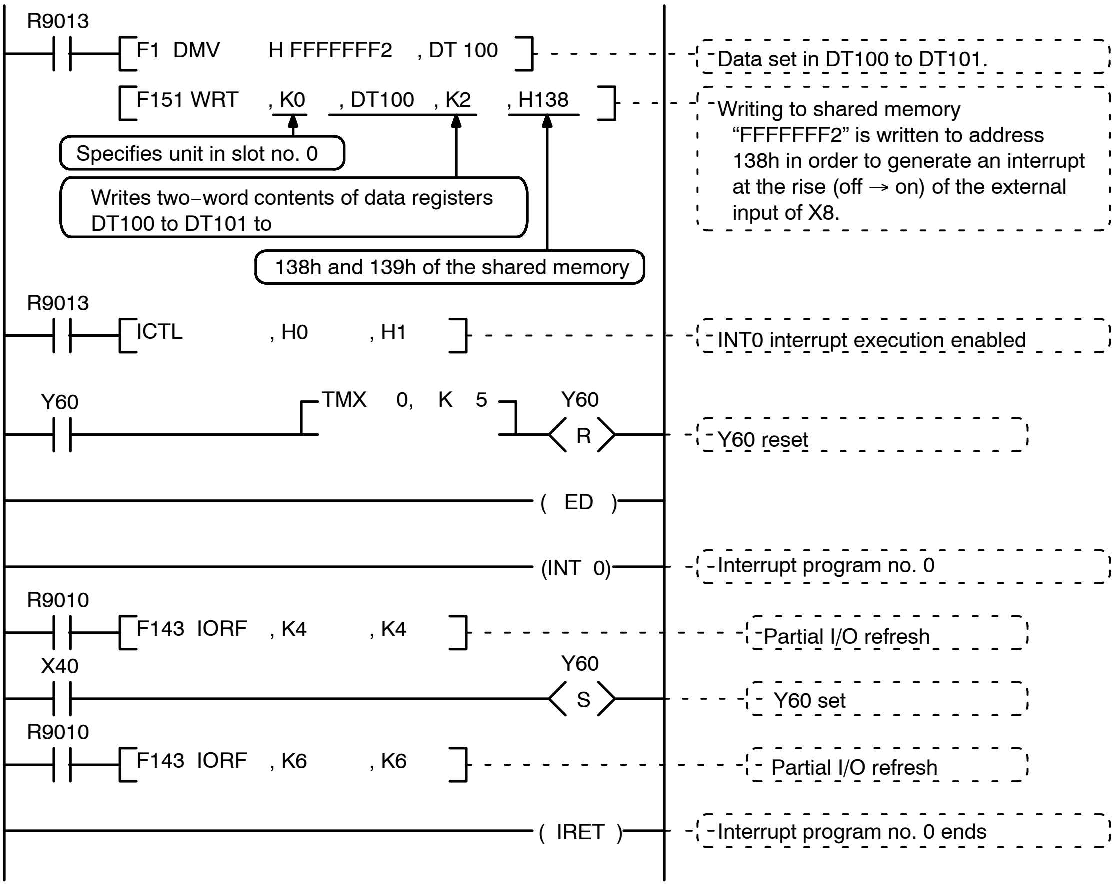
Setting of shared memory addresses 138h and 139h

(bit)	32			16	15			0
External input	XF	XE	XD	XC	XB	XA	X9	X8
Interrupt number	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
Set value	F	F	F	F	F	F	F	2
Interrupt Setting	Not used	Not used	Not used	Not used	Not used	Not used	Not used	off → on

7.2.5 Sample Program

The value “FFFFFFF2” is written to the interrupt setting area of the shared memory (138h and 139h), and the interrupt is set to occur at the rise (off → on) of the external input of X8.
The program here shows the interrupt being enabled prior to the end command, and the interrupt taking place subsequent to the end command.

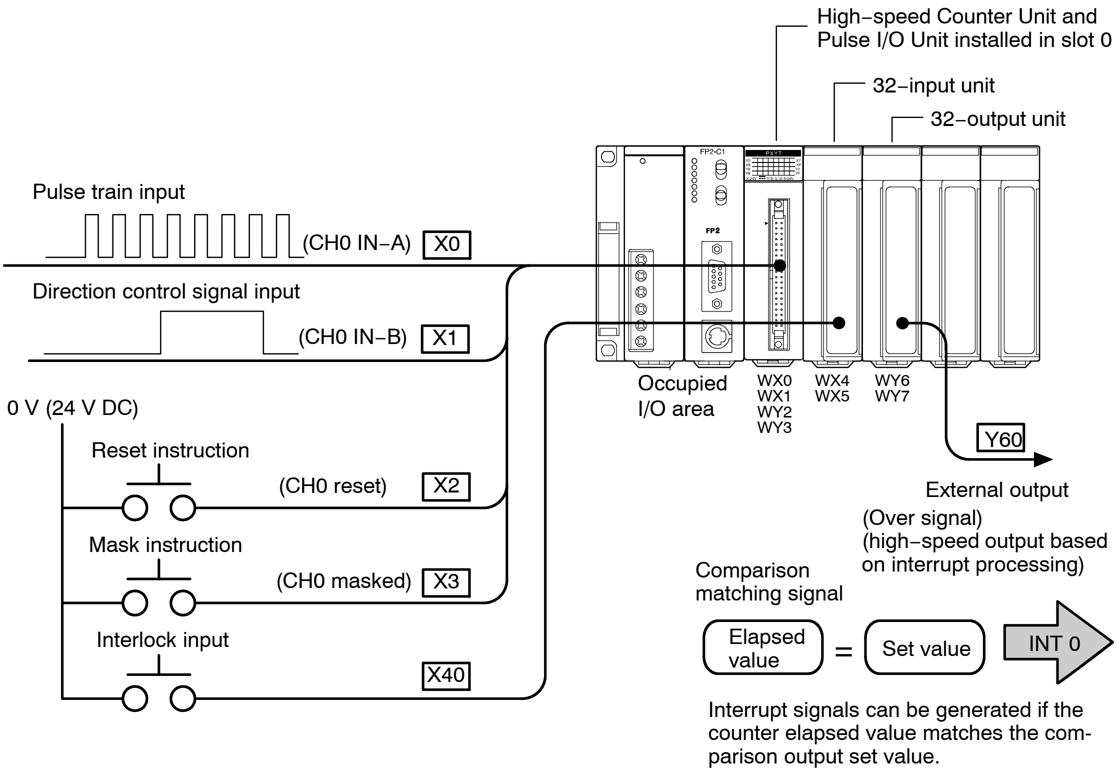
This program assumes that the FP2 High−speed Counter Unit/FP2 Pulse I/O Unit has been installed in slot 0.



When Mode C is used, please be aware that the interrupt signal will be INT16.

7.3 Using the Interrupt Function Based on Comparison Matching Signals

7.3.1 Overview

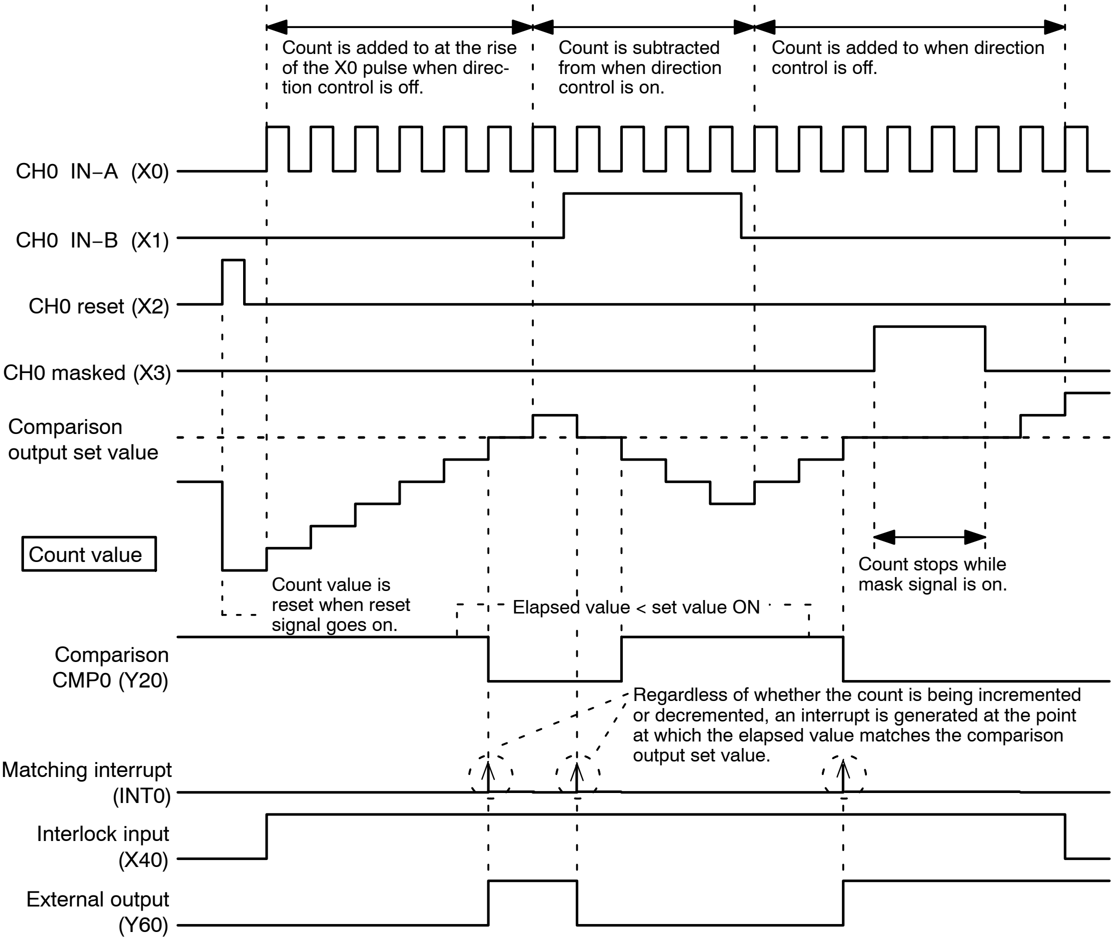


The pulse train is input to X0 and the direction control signal to X1, and the number of counts is calculated. Regardless of whether the count is being incremented or decremented, the number of pulses being counted is compared with a comparison output set value specified ahead of time, and if the value matches the preset value, the INT0 interrupt is generated. When INT0 is generated, the interrupt program is executed from the INT0 to the IRET of the sequence program, and the output of Y60 is output at high speed.

For information on the comparison function, see page 9 – 3.

7.3.2 Timing Chart

The following shows the changes in the count value and the output based on the input states of the various signals.

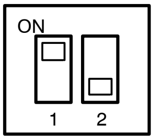


For information on the reset, mask, and other signals, see page 8 – 6.

7.3.3 Setting the Mode Setting Switches

Set the mode setting switches to Mode B, so that all eight interrupts from INT0 to INT7 can be used. If only one interrupt is needed per unit, the mode can be set to Mode C. When Mode C is used, the interrupt signal will be INT16.

Mode B (SW1 → on, SW2 → off)

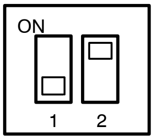


With Interruption (interrupt points: 8)

Up to eight interrupts can be used for each unit (INT0 to INT7).

When this mode is specified, eight interrupt points (INT0 to INT7) are automatically defined for the unit, regardless of whether or not the interrupt function is used.

Mode C (SW1 → off, SW2 → on)



Intelligent unit that generates interrupts (interrupt points: 1)

One interrupt for each unit becomes effective (INT0 *1).

INT1 to INT7 are invalid, even if interrupt settings have been defined for them.

*1: This INT0 defines the interrupt position for the unit. Interrupt program numbers that can be specified in the sequence program are INT16 to 23.

7.3.4 Shared Memory Settings

Interrupt Setting

If the interrupt function is being used, settings must be entered in the shared memory, in addition to setting the mode setting switches on the side panel of the main unit.
In the example, the INT0 interrupt is generated by CMP0, using the comparison output function, so a value of "FFFFFFF1" will be written to addresses 138h and 139h of the shared memory.

Setting of shared memory addresses 138h and 139h

(bit)	32			16	15			0
Interrupt number	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
Set value	F	F	F	F	F	F	F	1
Interrupt Setting	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CMP0

Counter Setting

This sets the operation modes for the various counter channels.
In the example shown here, the pulse train is input to X0 and the direction control signal to X1, and the counter function is used in the direction control mode, so a value of "FFFFFF00" should be written to addresses 100h and 101h of the shared memory.

Setting of shared memory addresses 100h and 101h

(bit)	32			16	15			0
External output	X7	X6	X5	X4	X3	X2	X1	X0
Counter number	CH3		CH2		CH1		CH0	
Setting item	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting
Set value	F	F	F	F	F	F	0	0
Counter setting	Not used	Not used	Not used	Not used	Not used	Not used	Direction control	Used

Setting the Comparison Output Set Value

A setting must be entered for the "comparison output set value", against which the counter elapsed value is compared.
In the example shown here, settings have been entered so that CMP0 is output when the counter elapsed value reaches 6, so "K6 (H6)" should be written to addresses 120h and 121h of the shared memory.

Setting of shared memory addresses 120h and 121h

(bit)	32			16	15			0
Setting item	Comparison output set value (for CMP0)							
Set value	0	0	0	0	0	0	0	6
Comparison output set value	K6							

Setting the Comparison Output

The counter CH number and output logic used in the comparison output function are selected.
In the example shown here, the counter elapsed value for CH0 is compared to the comparison output set value, and the comparison result is output to CMP0, so a value of “FFFFFFF0” should be written to addresses 104h and 105h of the shared memory.

Setting of shared memory addresses 104h and 105h

(bit)	32			16	15			0
Comparison output	CMP7	CMP6	CMP5	CMP4	CMP3	CMP2	CMP1	CMP0
Set value	F	F	F	F	F	F	F	0
Comparison output	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CH0 comparison

In the example shown here, the output logic from the CMP0 comparison output is set to go on if the elapsed value is smaller than the set value. To set this so that the output goes on if the elapsed value is larger than or equal to the set value, “FFFFFFF4” should be written to addresses 104h and 105h of the shared memory.

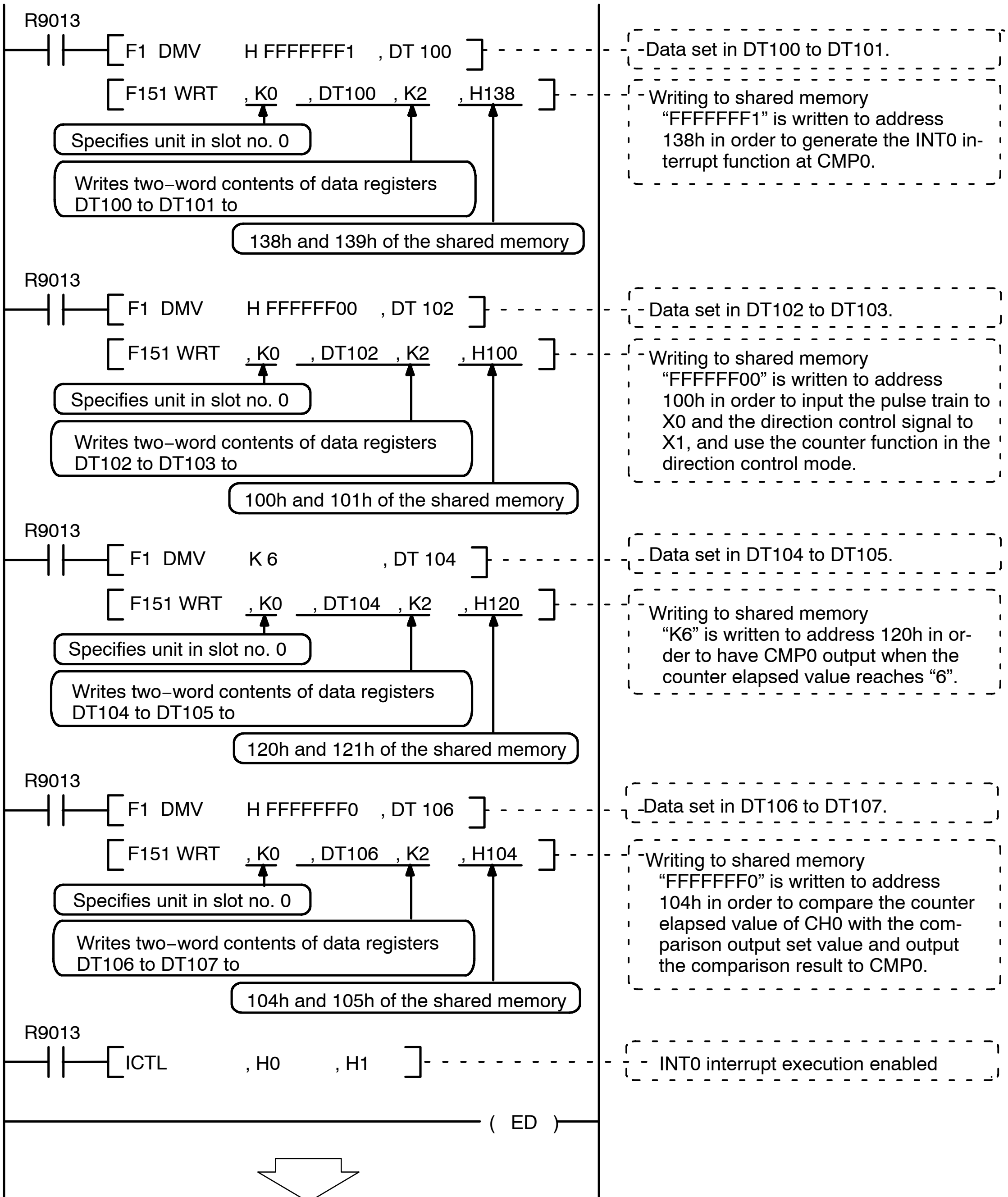
☞ **Note**

For the settings relating to comparison output, the comparison output set value should be set in the shared memory first. If both the counter initial value and the comparison output set value are “0”, entering the settings in the reversed order can cause matching output to be output at the point when the data is set.

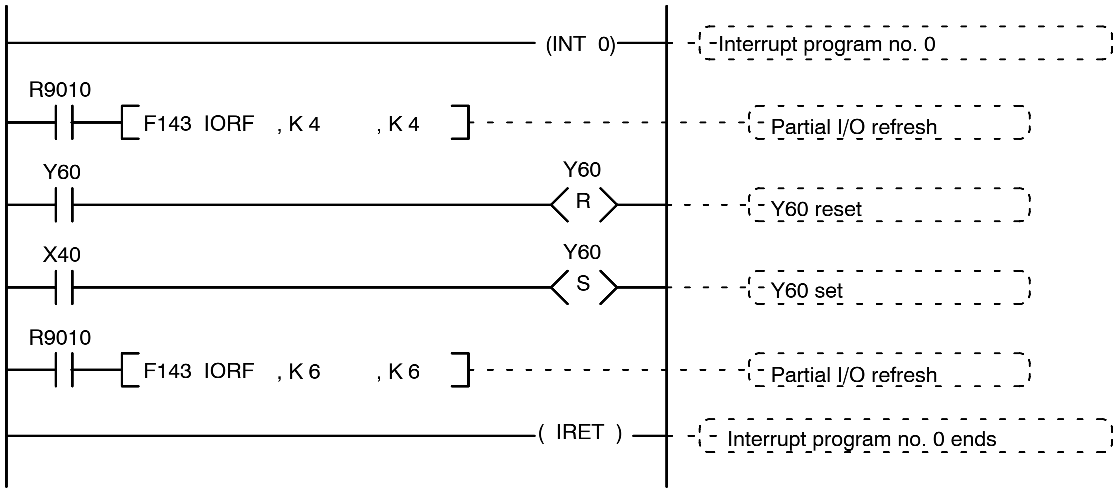
7.3.5 Sample Program

This shows settings relating to the interrupts, the counter mode, and the comparison output function being entered in the shared memory. The program is written so that it will be executed using an interrupt following the end command.

This program assumes that the FP2 High−speed Counter Unit or FP2 Pulse I/O Unit has been installed in slot 0.



next page


(INT 0)
Interrupt program no. 0
R9010
F143 IORF , K 4 , K 4
Partial I/O refresh
Y60
Y60
R
Y60 reset
X40
Y60
S
Y60 set
R9010
F143 IORF , K 6 , K 6
Partial I/O refresh
(IRET)
Interrupt program no. 0 ends

7.3 Using the Interrupt Function Based on Comparison Matching Signals

Chapter 8

Using the Counter Function

☛ next page

8.1 About the Counter Function

8.1.1 What is the Counter Function?

The counter function is a function in which the number of pulses input is counted and is reflected in the elapsed value. Also, data can be written to the elapsed value to specify offset values.

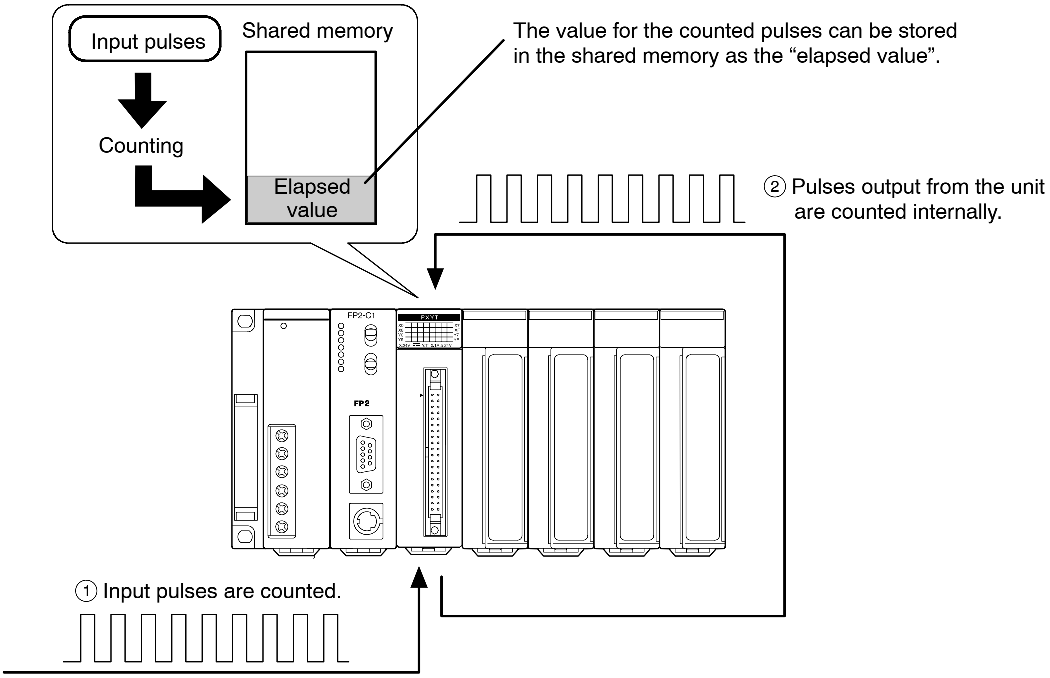
The FP2 High−speed Counter Unit/FP2 Pulse I/O Unit has two pairs of input counters, with four channels. There are three types of paired input modes:

- Direction control mode
- Individual input mode
- Phase input mode

As a feature of the FP2 High−speed Counter Unit and FP2 Pulse I/O Unit, the connection destination (condition) for the counted pulse signals can be selected.

① Input from the I/O connector can be counted.

② Pulses generated in the pulse output function or PWM output function can be connected internally and counted.



8.1.2 Entering Settings for the Counter Function

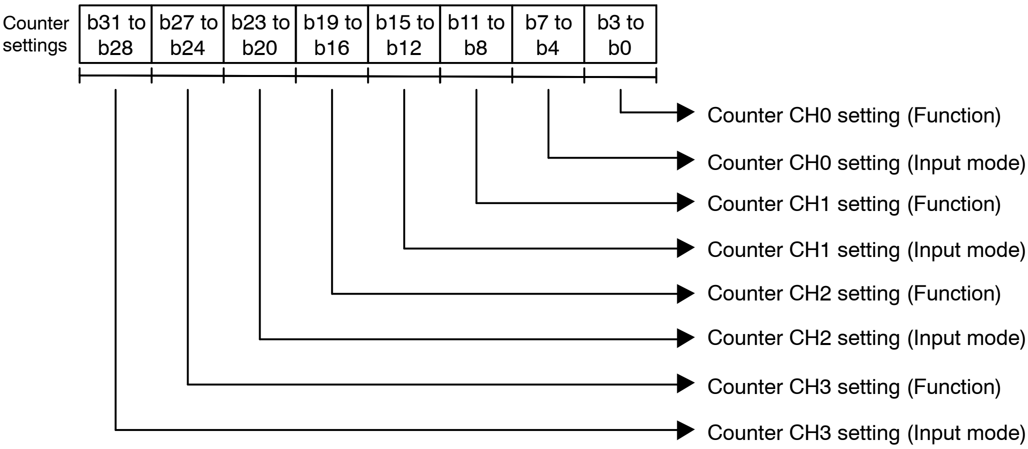
Settings must be entered in the shared memory in order to use the counter function.

In addition to the shared memory settings, the counter can also be masked or reset using counter control signals.

Procedure 1: Shared memory settings

The settings in the shared memory specify the operation modes for the various counter channels.
The counter function mode settings should be entered as shown below.

Addresses: 100 h, 101h



Settings

Input mode (effective only for terminal input)

Set value (HEX)	Function	
	Terminal input mode	Multiplier
0	Direction control *3	None
1	Individual input	
2	Phase input	Multiplied once
3		Multiplied twice
4		Multiplied four times
5	Invalid *2	
6		
7		
8		
9		
A		
B		
C		
D		
E		
F		

Functions

Set value (HEX)	Function
	Counter
0	Used (Terminal input)
1	
2	Used (Internal connection) *1
3	
4	Invalid *2
5	
6	
7	
8	
9	
A	
B	
C	
D	
E	
F	Not used *3

*1: Used when pulse output and PWM output are internally connected and the number of pulses output are counted.
*2: This setting should not be used.
*3: When the power supply is turned on, the default setting for the input mode is “Direction control”, and for the function settings is “Not used”.

Notes

- **The shared memory should always be accessed in two–word units.**
- **With the internal connection to the pulse output and PWM output counters, the channels corresponding to the pulse output counter, and to the PWM output counter, are fixed.**
- **When the pulse output and PWM output are internally connected to the counter, the counter input mode is automatically set to a mode that matches the pulse output and PWM output. Please be aware that, for this reason, the counter input mode specified ahead of time will be ignored.**

◆ REFERENCE

For information on shared memory addresses, see page 13 – 12.

Procedure 2: Counter control signals

With the counter function, counter control signals can be used to mask or reset items.

There are two types of counter control signals, described below: control based on external input terminals, and control based on programming. Either type can be used for counter control.

Control based on external input terminals

Table of control signals (external input terminals)

External terminal	Input allocation	Function		
		Target counter	Control content	
A3	X2	CH0	Reset	Counter elapsed value is reset to 0 when input goes on.
A4	X3		Mask	Counter operation is temporarily stopped when input goes on.
A7	X6	CH1	Reset	Counter elapsed value is reset to 0 when input goes on.
A8	X7		Mask	Counter operation is temporarily stopped when input goes on.
B3	XA	CH2	Reset	Counter elapsed value is reset to 0 when input goes on.
B4	XB		Mask	Counter operation is temporarily stopped when input goes on.
B7	XE	CH3	Reset	Counter elapsed value is reset to 0 when input goes on.
B8	XF		Mask	Counter operation is temporarily stopped when input goes on.

Control based on programming

Table of control signals (internal output terminals)

Output allocation	Function		
	Target counter	Control content	
Y30	CH0	Reset	Counter elapsed value is reset to 0 when output goes on.
Y31		Mask	Counter operation is temporarily stopped when output goes on.
Y32	CH1	Reset	Counter elapsed value is reset to 0 when output goes on.
Y33		Mask	Counter operation is temporarily stopped when output goes on.
Y34	CH2	Reset	Counter elapsed value is reset to 0 when output goes on.
Y35		Mask	Counter operation is temporarily stopped when output goes on.
Y36	CH3	Reset	Counter elapsed value is reset to 0 when output goes on.
Y37		Mask	Counter operation is temporarily stopped when output goes on.

☞ **Note**

When the counter is connected internally, please be aware that control input from the I/O connector (control based on external terminals) will be ignored.

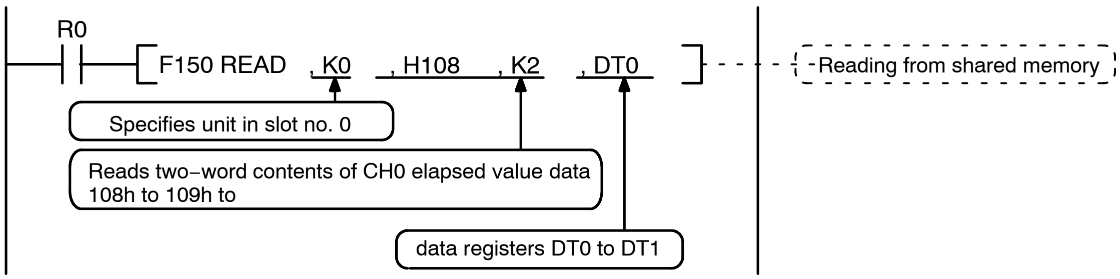
8.1.3 Reading the Counter Elapsed Values

The elapsed values for the various counters are stored in the shared memory.

To read elapsed values, use the F150 (READ) instruction and P150 (PREAD) instruction (these read data from intelligent units), and read the values in two–word units.

	Addresses	Range
Counter CH0 elapsed values	108h, 109h	K–2, 147, 483, 648 to K+2, 147, 483, 647
Counter CH1 elapsed values	10Ah, 10Bh	K–2, 147, 483, 648 to K+2, 147, 483, 647
Counter CH2 elapsed values	10Ch, 10Dh	K–2, 147, 483, 648 to K+2, 147, 483, 647
Counter CH3 elapsed values	10Eh, 10Fh	K–2, 147, 483, 648 to K+2, 147, 483, 647

The following example shows the elapsed values for the counter CH0 being read using the F150 (READ) instruction, and stored in DT0.



8.1.4 Writing the Counter Elapsed Values

The elapsed values for the various counters are stored in the shared memory.

To write elapsed values, use the F151 (WRT) instruction and P151 (PWRT) instruction (these write data to intelligent units), and write the values in two−word units.

Addresses: 108h, 109h

Counter CH0 elapsed values: K–2, 147, 483, 648 to K+2, 147, 483, 647

Addresses: 10Ah, 10Bh

Counter CH1 elapsed values: K–2, 147, 483, 648 to K+2, 147, 483, 647

Addresses: 10Ch, 10Dh

Counter CH2 elapsed values: K–2, 147, 483, 648 to K+2, 147, 483, 647

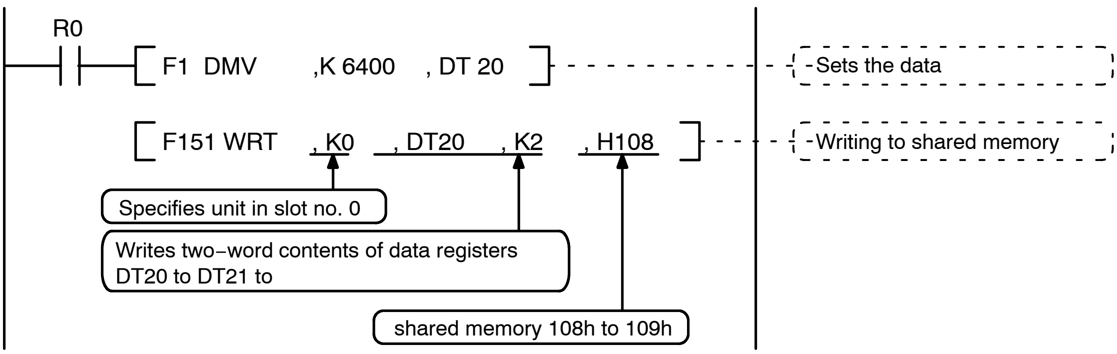
Addresses: 10Eh, 10Fh

Counter CH3 elapsed values: K–2, 147, 483, 648 to K+2, 147, 483, 647

Tip

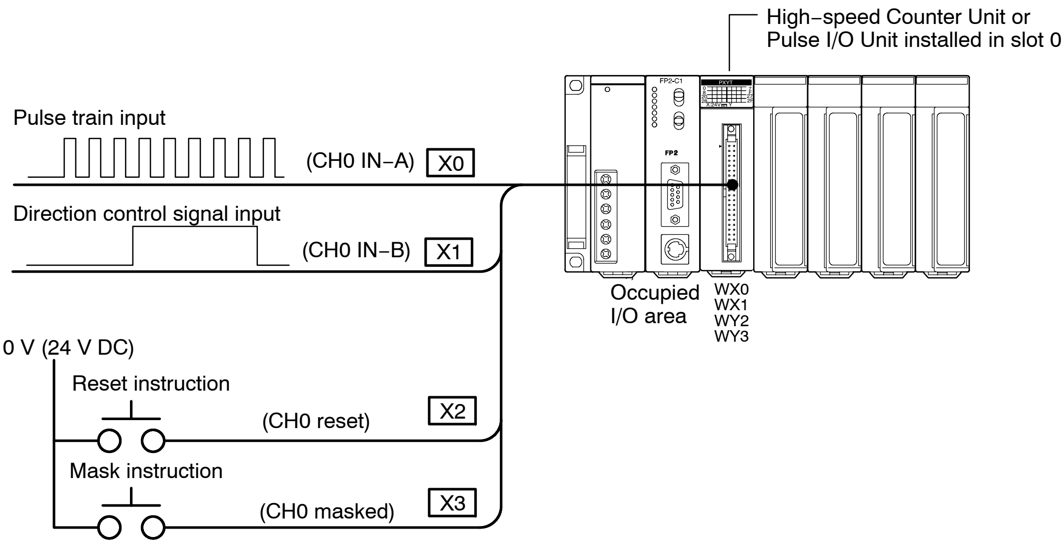
Offset values for counters can be specified by writing counter elapsed values.

The following example shows the F151 (PWRT) instruction being used to write the written data stored in DT20 to the elapsed value of the counter CH0.



8.2 Using the Counter Function in the Direction Control Mode

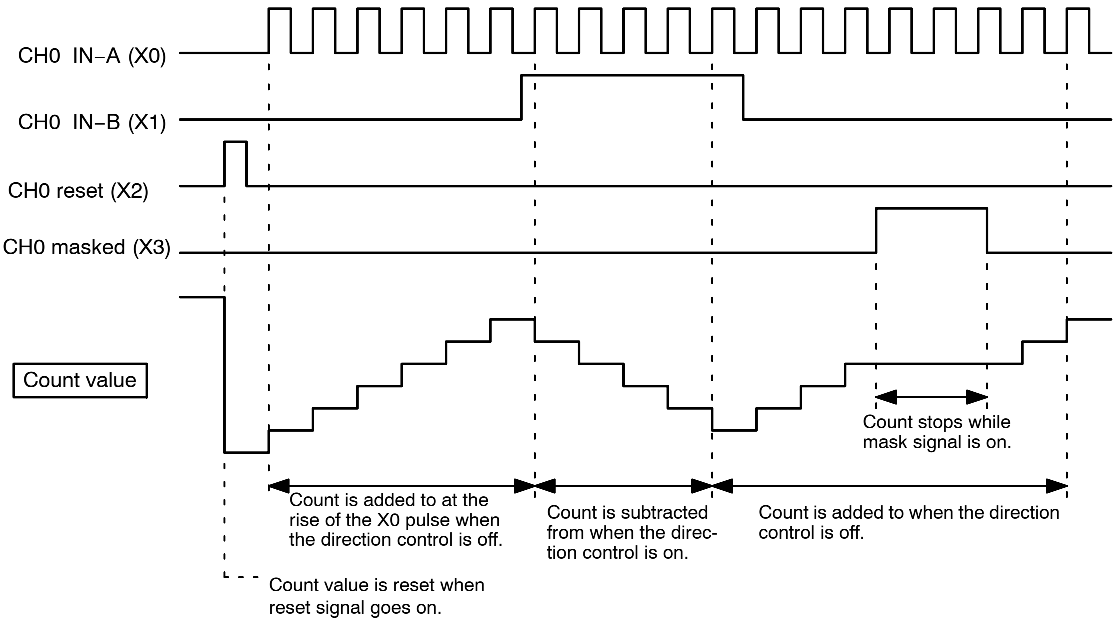
8.2.1 Overview



The pulse train is input to X0 and the direction control signal to X1, and the number of counts is calculated. The X2 Reset instruction resets the counter elapsed values, and the X3 Mask instruction temporarily stops the counting operation.

8.2.2 Timing Chart

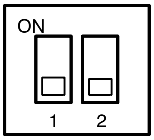
Changes in the counted values based on the input states of the various signals are shown below. The counted value changes at the rise of the pulse input.



8.2.3 Setting the Mode Setting Switches

Specify Mode A to use only the counter function, without using interrupts.

Mode A (SW1 → off, SW2 → off)



No interruption

When this setting is used, the interrupt function will not operate even if used.

The counter function can be used regardless of whether the interrupt function is set to “Used” or “Not Used”.

8.2.4 Shared Memory Settings

Counter Setting

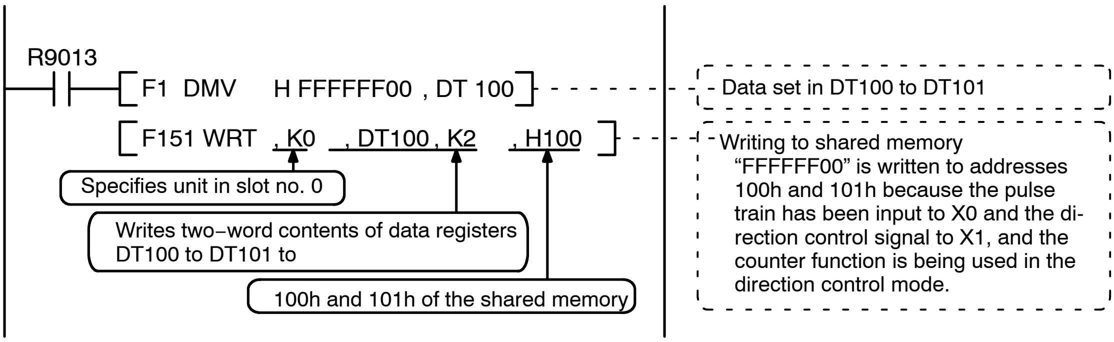
This sets the operation modes for each counter channels.
In the example shown here, the pulse train is input to X0 and the direction control signal to X1, and the counter function is used in the direction control mode, so a value of “FFFFFF00” should be written to addresses 100h and 101h of the shared memory.

Setting of shared memory addresses 100h and 101h

(bit)	32			16	15			0
External input	XD	XC	X9	X8	X5	X4	X1	X0
Counter number	CH3		CH2		CH1		CH0	
Setting item	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting
Set value	F	F	F	F	F	F	0	0
Counter setting	Not used	Not used	Not used	Not used	Not used	Not used	Direction control	Terminal input

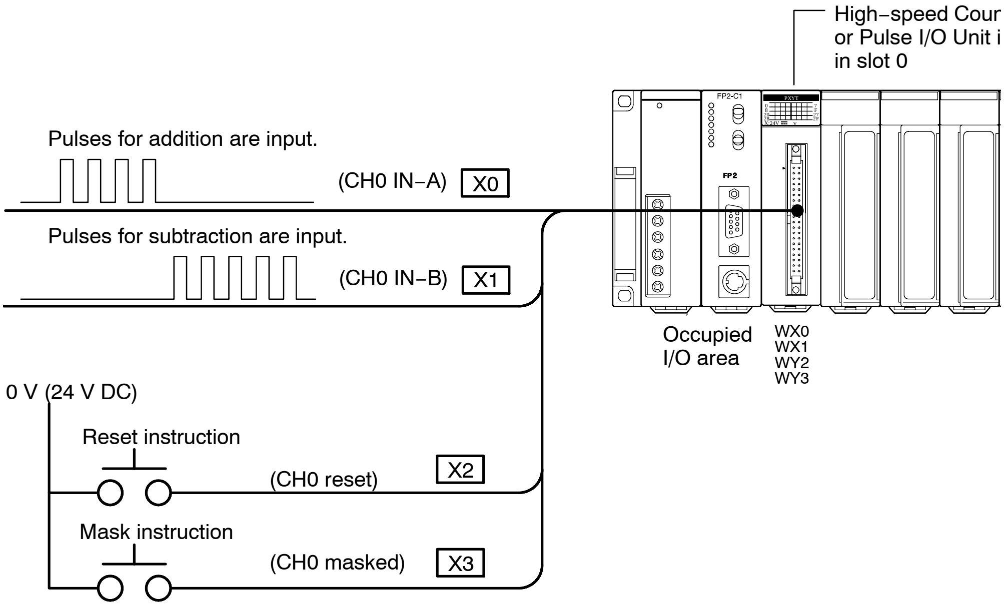
8.2.5 Sample Program

This program writes the value “FFFFFF00” to the counter setting area (100h, 101h) of the shared memory, inputs a pulse train to X0 and a direction control signal to X1, and sets the counter function to be used in the direction control mode.



8.3 Using the Counter Function in the Individual Input Mode

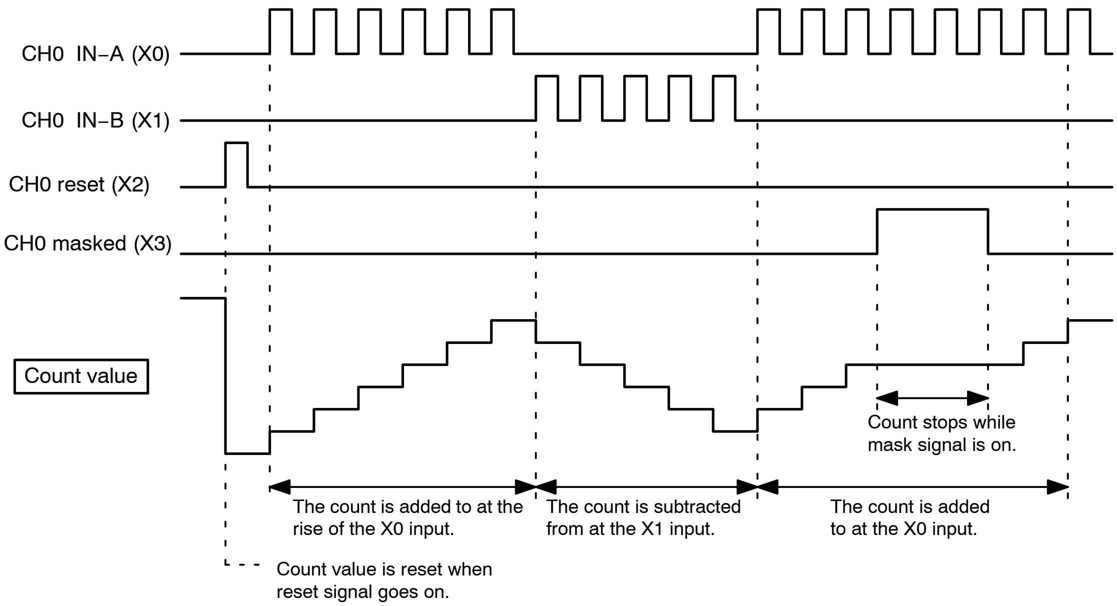
8.3.1 Overview



The pulses for addition are input to X0 and the pulses for subtraction to X1, and the number of pulses is counted. The X2 Reset instruction resets the counter elapsed values, and the X3 Mask instruction temporarily stops the counting operation.

8.3.2 Timing Chart

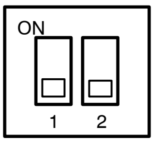
Changes in the counted values based on the input states of the various signals are shown below. The counted value changes at the rise of the various signals.



8.3.3 Setting the Mode Setting Switches

Specify Mode A to use only the counter function, without using interrupts.

Mode A (SW1 → off, SW2 → off)



No interruption

When this setting is used, the interrupt function will not operate even if used.

The counter function can be used regardless of whether the interrupt function is set to “Used” or “Not Used”.

8.3.4 Shared Memory Settings

Counter Setting

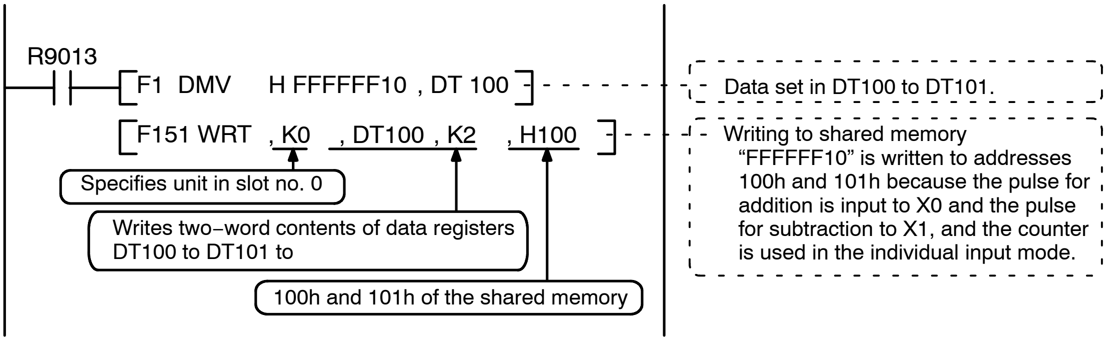
This sets the operation modes for each counter channels.
In this example, the pulse train for addition is input to X0 and the pulse train for subtraction to X1, and the counter function is used in the individual input mode. Therefore, a value of “FFFFFF10” should be written to addresses 100h and 101h of the shared memory.

Setting of shared memory addresses 100h and 101h

(bit)	32			16	15			0
External input	XD	XC	X9	X8	X5	X4	X1	X0
Counter number	CH3		CH2		CH1		CH0	
Setting item	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting
Set value	F	F	F	F	F	F	1	0
Counter setting	Not used	Not used	Not used	Not used	Not used	Not used	Individual input	Terminal input

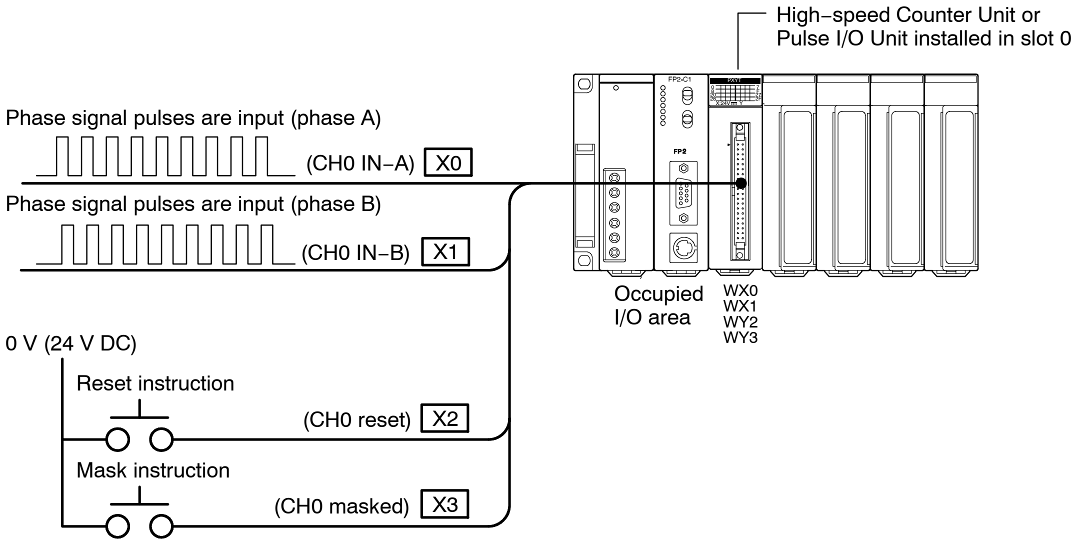
8.3.5 Sample Program

This program shows the value “FFFFFF10” being written to the counter setting area (100h, 101h) of the shared memory, the pulse for addition being written to X0, the pulse for subtraction being written to X1, and the counter function set to be used in the individual input mode.



8.4 Using the Counter Function in the Phase Input Mode

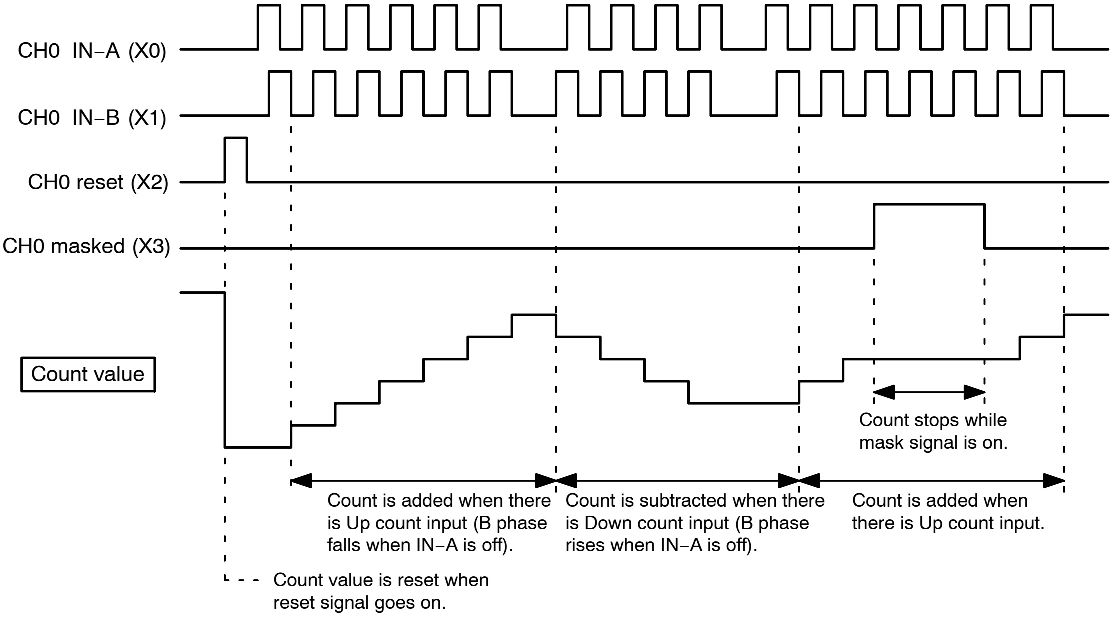
8.4.1 Overview



The phase signals for the encoder or other devices are input to X0 and X1, and the number input is counted. The X2 Reset instruction resets the counter elapsed values, and the X3 Mask instruction temporarily stops the counting operation.

8.4.2 Timing Chart

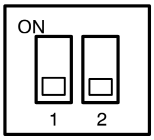
Changes in the counted values based on the input states of the various signals are shown below. When used with one multiplier, the counter values are added at the timing at which IN−B falls when IN−A is off, and are subtracted at the timing at which IN−B rises when IN−A is off.



8.4.3 Setting the Mode Setting Switches

Specify Mode A to use only the counter function, without using interrupts.

Mode A (SW1 → off, SW2 → off)



No interruption

When this setting is used, the interrupt function will not operate even if used.

The counter function can be used regardless of whether the interrupt function is set to “Used” or “Not Used”.

8.4.4 Shared Memory Settings

Counter Setting

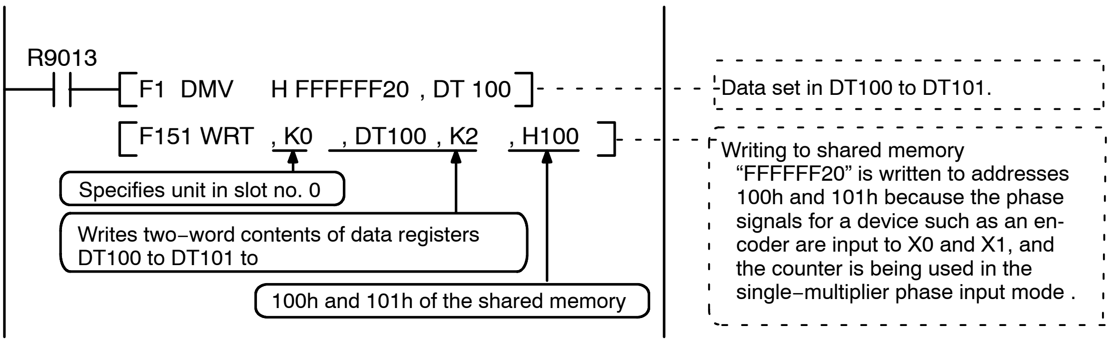
This sets the operation modes for the various counter channels.
In this example, phase signals for a device such as an encoder are input to X0 and X1, and the counter function is being used in the single−multiplier phase input mode, so the value “FFFFFF20” should be written to addresses 100h and 101h of the shared memory.

Setting of shared memory addresses 100h and 101h

(bit)	32			16	15			0
External input	XD	XC	X9	X8	X5	X4	X1	X0
Counter number	CH3		CH2		CH1		CH0	
Setting item	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting
Set value	F	F	F	F	F	F	2	0
Counter setting	Not used	Not used	Not used	Not used	Not used	Not used	Phase input	Terminal input

8.4.5 Sample Program

In this program, “FFFFFF20” is written to the counter setting area (100h, 101h) of the shared memory, the phase signals for a device such as an encoder are input to X0 and X1, and the counter function is set to be used in the single−multiplier phase input mode.



Tip

The phase differential input mode has the doubling multiplier function, in which the count value for input pulses can be multiplied. For detailed information, see page 1 – 9.

8.4 Using the Counter Function in the Phase Input Mode

Chapter 9

Using the Comparison Output Function

9.1 About the Comparison Output Function

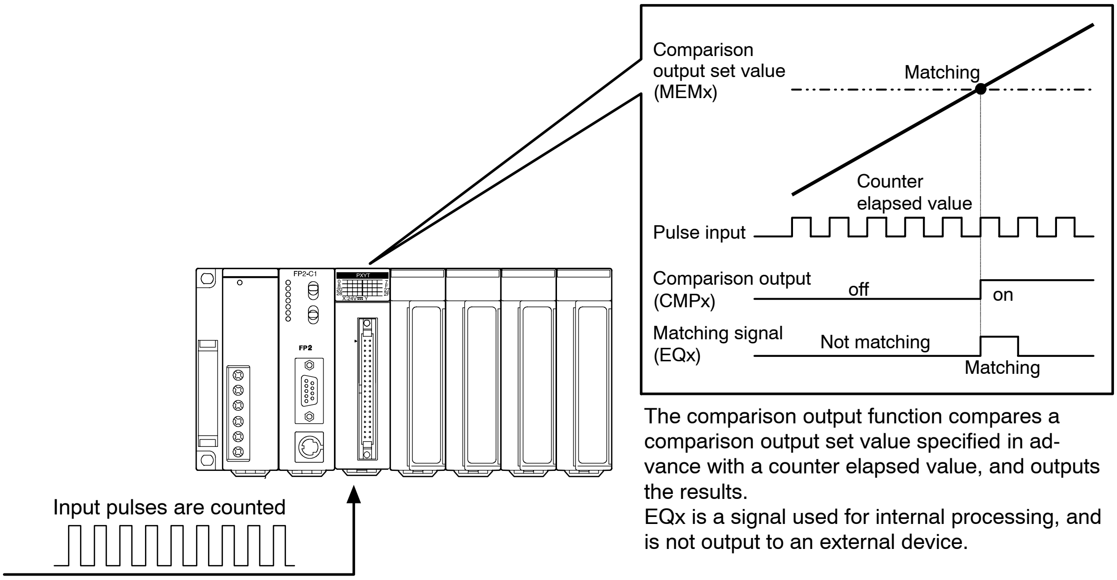
9.1.1 What is the Comparison Output Function?

The comparison output function compares a comparison output set value against a counter elapsed value, and outputs the results of the comparison.

Comparison result output [CMPx]: Comparison output set value ≦ Counter elapsed value

Either “on if elapsed value ≧ set value” or “on if elapsed value < set value” can be selected for the comparison result output.

With the FP2 High−speed Counter Unit and FP2 Pulse I/O Unit, eight comparison output set values can be set, and the counter channels used to compare these can be freely selected by the user. This makes it possible to carry out comparisons on up to eight levels, by setting all of the comparison output set values to the same counter.



The comparison output function compares a comparison output set value specified in advance with a counter elapsed value, and outputs the results.
EQx is a signal used for internal processing, and is not output to an external device.

9.1.2 Entering Settings for the Comparison Output Function

To use the comparison output function, a comparison output set value must be entered in the shared memory (Procedure 1), and comparison output settings must be entered in the shared memory (Procedure 2).

Procedure 1: Setting the comparison output set value in the shared memory

The comparison output set value that is compared against the counter elapsed value must be specified.

Comparison output set value (for CMP0)	MEM0	Addresses: 120h, 121h	K–2, 147, 483, 648 to K+2, 147, 483, 647
Comparison output set value (for CMP1)	MEM1	Addresses: 122h, 123h	K–2, 147, 483, 648 to K+2, 147, 483, 647
Comparison output set value (for CMP2)	MEM2	Addresses: 124h, 125h	K–2, 147, 483, 648 to K+2, 147, 483, 647
Comparison output set value (for CMP3)	MEM3	Addresses: 126h, 127h	K–2, 147, 483, 648 to K+2, 147, 483, 647
Comparison output set value (for CMP4)	MEM4	Addresses: 128h, 129h	K–2, 147, 483, 648 to K+2, 147, 483, 647
Comparison output set value (for CMP5)	MEM5	Addresses: 12Ah, 12Bh	K–2, 147, 483, 648 to K+2, 147, 483, 647
Comparison output set value (for CMP6)	MEM6	Addresses: 12Ch, 12Dh	K–2, 147, 483, 648 to K+2, 147, 483, 647
Comparison output set value (for CMP7)	MEM7	Addresses: 12Eh, 12Fh	K–2, 147, 483, 648 to K+2, 147, 483, 647

Note

The shared memory should always be accessed in two−word units.

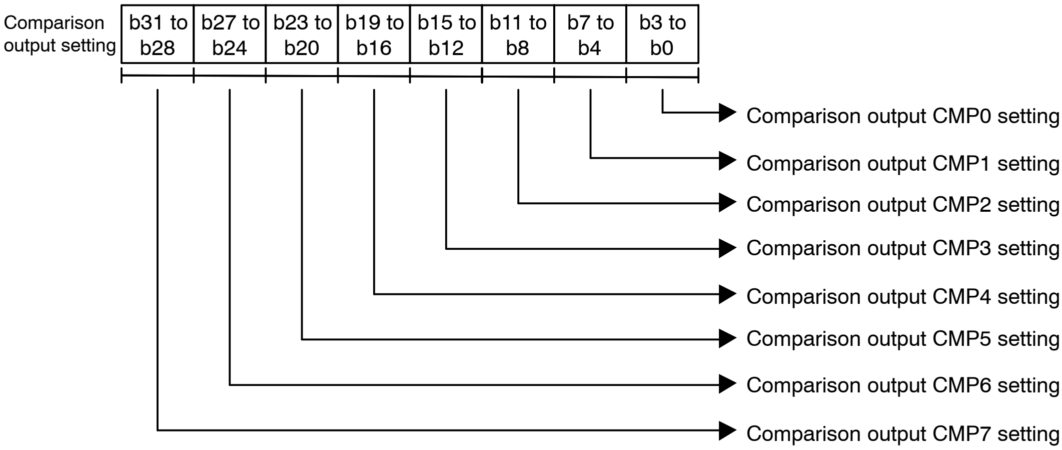
◆ REFERENCE

For information on shared memory addresses, see page 13 – 12.

Procedure 2: Setting the comparison output settings in the shared memory

Select the counter channel and the output logic used to compare the comparison output set value.

Addresses: 104 h, 105h



Comparison output setting

Set value (HEX)	Function		
	Comparison output function	Output logic	Counter CH used for comparison
0	Used	on if elapsed value < set value	CH0
1			CH1
2			CH2
3			CH3
4		on if elapsed value ≧ set value	CH0
5			CH1
6			CH2
7			CH3
8	Invalid *1	Invalid *1	
9			
A			
B			
C			
D			
E			
F	Not used *2	—	

*1: No settings should be entered.
*2: When the power supply is turned on, the default value of “Not used” is set for this.

☛ next page

Notes

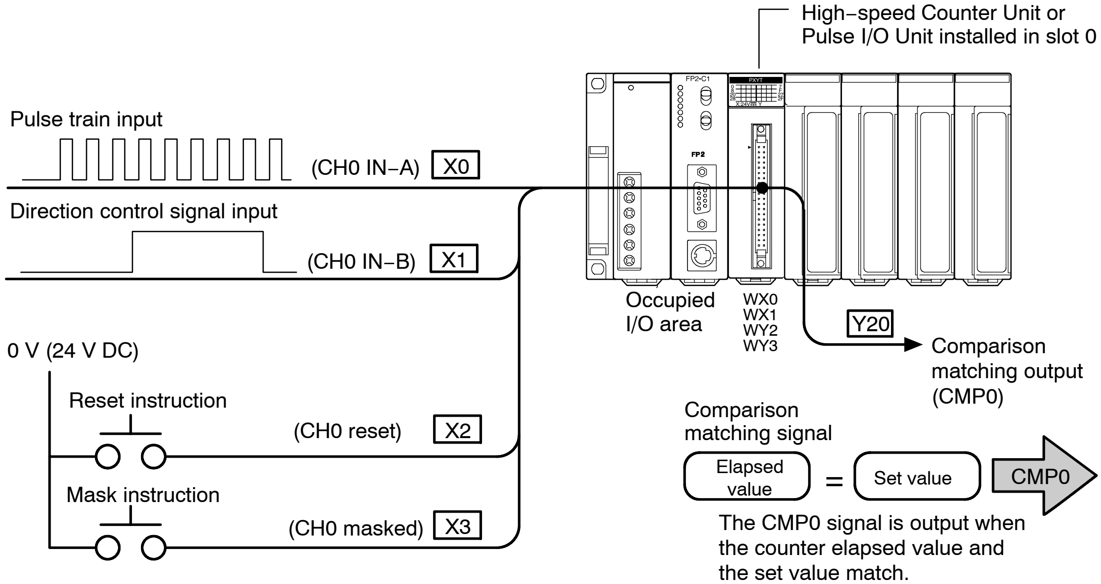
- **The shared memory should always be accessed in two−word units.**
- **Please be aware that if this setting is being used, regardless of whether or not the counter function is used, the comparison output set value is compared to the counter elapsed value.**
- **When setting the comparison output in the shared memory first specify the comparison output set value. Please be aware that, if both the counter initial value and the comparison output set value are a value such as “0”, entering the settings in the reversed order can cause matching output to be output at the point when the data is set.**

◆ **REFERENCE**

For information on shared memory addresses, see page 13 – 12.

9.2 Using the Comparison Output Function with the Counter

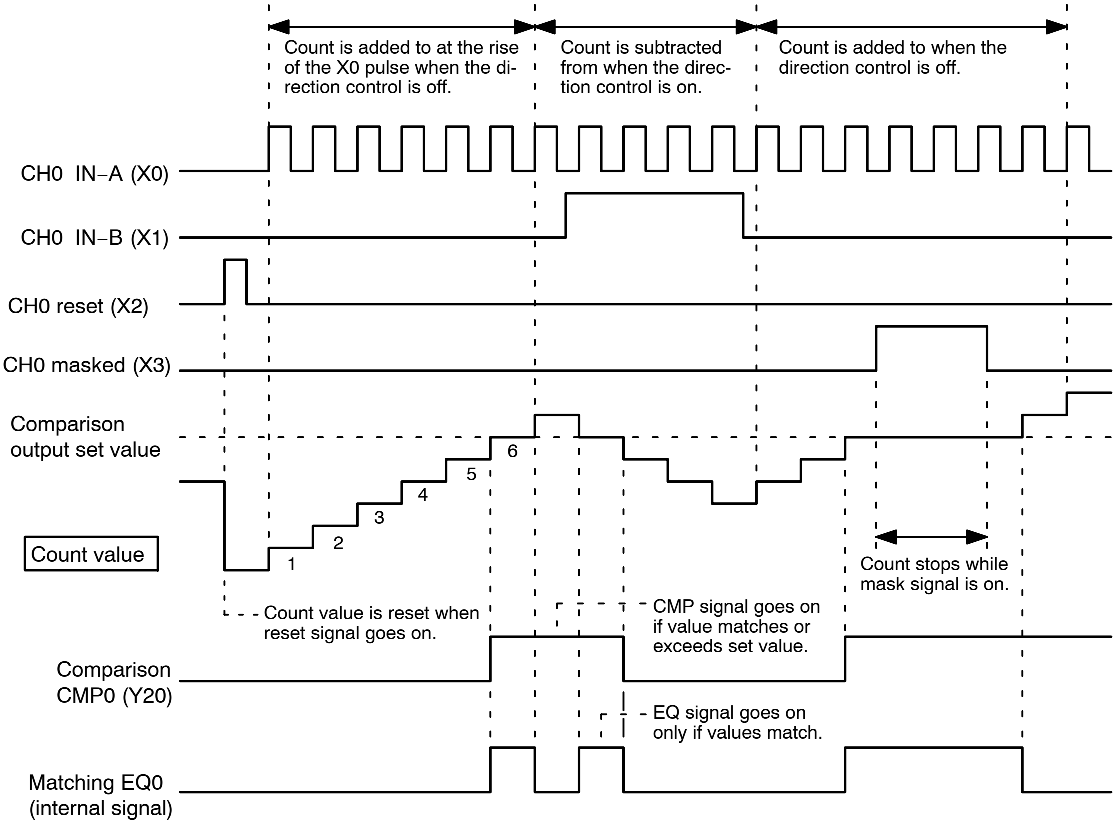
9.2.1 Overview



The comparison output function compares the comparison output set value set in advance with the counter elapsed value, and outputs the results. This counter operates in any mode. The example on this section shows the counter being used in the direction control mode.

9.2.2 Timing Chart

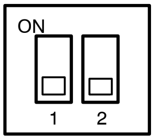
The following shows the changes in the count value and the output based on the input states of the various signals.



9.2.3 Setting the Mode Setting Switches

Specify Mode A to use only the counter function, without using interrupts.

Mode A (SW1 → off, SW2 → off)



No interruption

When this setting is used, the interrupt function will not operate even if used.

The counter function can be used regardless of whether the interrupt function is set to “Used” or “Not Used”.

9.2.4 Shared Memory Settings

Counter Setting

This sets the operation modes for the various counter channels.
In the example shown here, the pulse train is input to X0 and the direction control signal to X1, and the counter function is used in the direction control mode, so a value of “FFFFFF00” should be written to addresses 100h and 101h of the shared memory.

Setting of shared memory addresses 100h and 101h

(bit)	32			16	15			0
External output	XD	XC	X9	X8	X5	X4	X1	X0
Counter number	CH3		CH2		CH1		CH0	
Setting item	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting
Set value	F	F	F	F	F	F	0	0
Setting contents	Not used	Not used	Not used	Not used	Not used	Not used	Direction control	Terminal input

Setting the Comparison Output Set value

Here, the comparison output set value, which is compared to the counter elapsed value, is set.
In the example shown here, the value is set so that CMP0 is output when the counter elapsed value reaches “6”. To do this, write a value of “K6 (H6)” to addresses 120h and 121h of the shared memory.

Setting of shared memory addresses 120h and 121h

(bit)	32			16	15			0
Setting item	Comparison output set value (for CMP0)							
Set value	0	0	0	0	0	0	0	6
Setting contents	K6							

Comparison Output Setting

The channel number and output logic for the counter used in the comparison output function are selected.
In the example shown here, the value of “FFFFFFF4” should be written to addresses 104h and 105h of the shared memory, so that the elapsed value of the CH0 counter will be compared with the comparison output set value, and the result output to CMP0.

Setting contents of shared memory addresses 104h and 105h

(bit)	32			16	15			0
Comparison output	CMP7	CMP6	CMP5	CMP4	CMP3	CMP2	CMP1	CMP0
Set value	F	F	F	F	F	F	F	4
Setting contents	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CH0 comparison*

* Goes on if the elapsed value is more than or equal to the set value.

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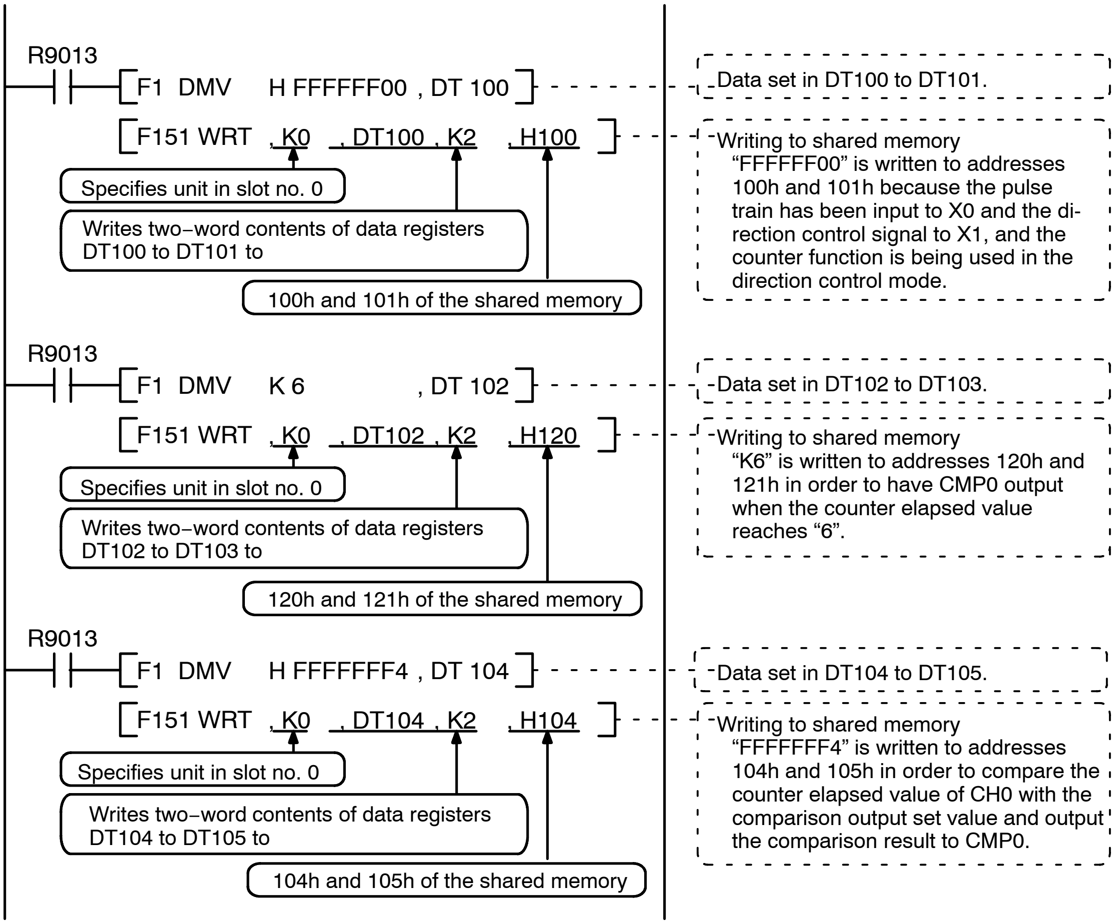
☞ **Note**

When settings the comparison output in the shared memory first specify the comparison output set value. Please be aware that, if both the counter initial value and the comparison output set value are a value such as “0”, entering the settings in the reversed order can cause matching output to be output at the point when the data is set.

9.2.5 Sample Program

This program shows the counter mode setting and settings concerning the comparison output function being entered in the shared memory.



9.2 Using the Comparison Output Function with the Counter

Chapter 10

Using the Pulse Output Function (Only for the Pulse I/O Unit)

☛ next page

10.1 About the Pulse Output Function

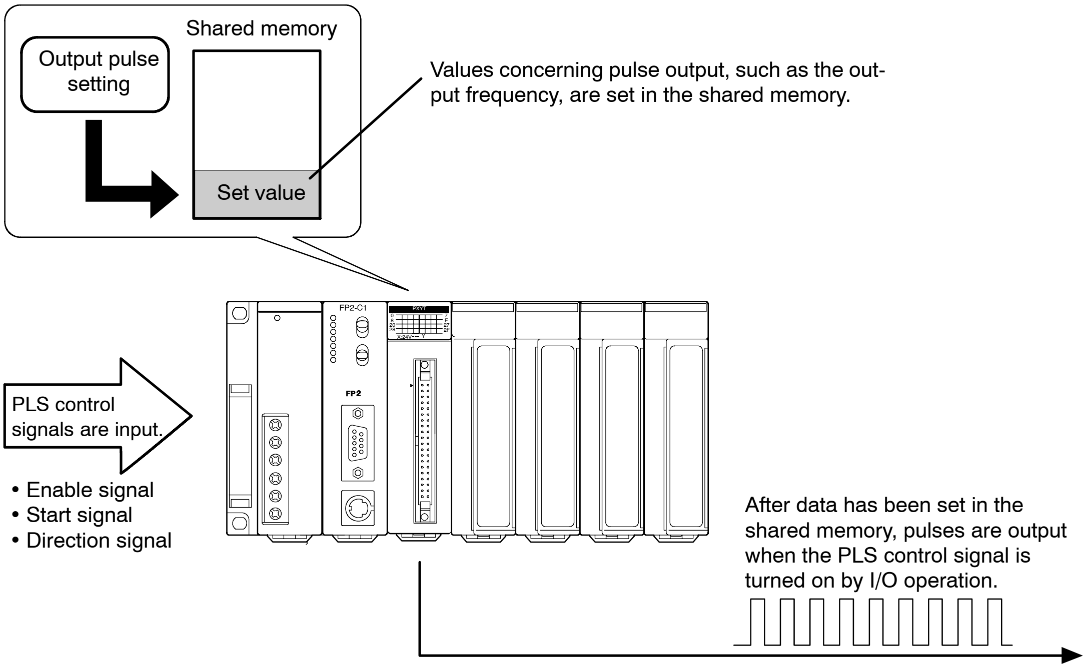
10.1.1 What is the Pulse Output Function?

The pulse output function outputs any desired frequency within a range of 1 Hz to 100 kHz. Settings are entered in units of 1 Hz.

Two modes are available for the output format.

- Direction control
- Individual output

Also, the FP2 Pulse I/O Unit can output pulses on up to four channels. Because the pulse output function and the PWM output function can both be selected, however, there will be fewer channels available for use with the pulse output function if the PWM output function is also being used.



Note

The four channels listed below are used for pulse−related output (pulse output and PWM output):

– Channel 0: PLS0 output or PWM0 output

– Channel 1: PLS1 output or PWM1 output

– Channel 2: PLS2 output or PWM2 output

– Channel 3: PLS3 output or PWM3 output

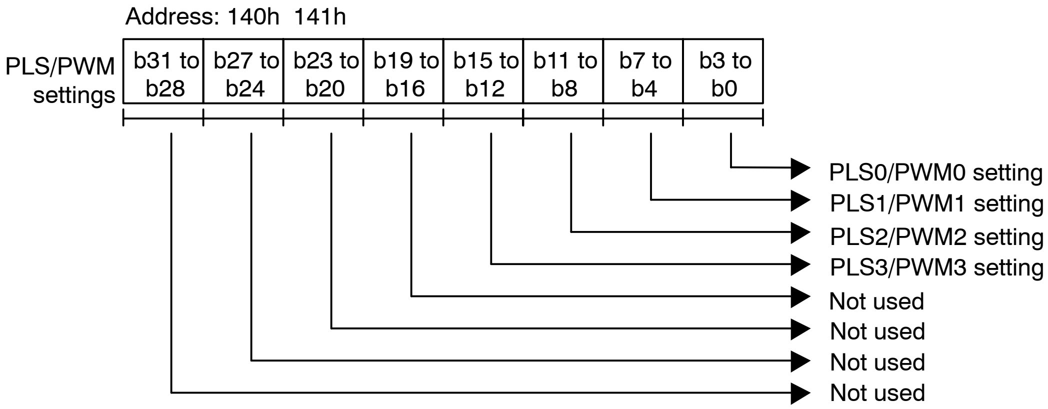
10.1.2 Entering Settings for the Pulse Output Function

Using the pulse output function involves entering PLS/PWM settings in the shared memory (Procedure 1), and setting the PLS/PWM frequency settings in the shared memory (Procedure 2).

In addition to the shared memory settings, control of the Enable, Start and Direction signals is necessary using the PLS control signal.

Procedure 1: PLS/PWM settings in the shared memory

The pulse output type should be specified using the PLS/PWM setting in the shared memory. The same applies if PWM output is selected as the pulse function.



Pulse output settings (PWM, PLS)

Set value (HEX)	Function		
	Pulse function	**Timing at which data changes**	**Output mode**
0	PWM	Updated at rise of PLSx start signal	—
1		At rise of PLSx start signal, or on comparison output	
2		At rise of PLSx start signal, or when data is updated	
3		Reserved as spare	
4	PLS	Updated at rise of PLSx start signal	Direction control
5			Individual output
6		At rise of PLSx start signal, or on comparison output	Direction control
7			Individual output
8		At rise of PLSx start signal, or when data is updated	Direction control
9			Individual output
A	Invalid *1	Invalid *1	Invalid *1
B			
C			
D			
E			
F	Not used *2	—	—

*1: No settings should be entered.
*2: When the power supply is turned on, the default value of "Not used" is set for this.

Note

The shared memory should always be accessed in two-word units.

◆ REFERENCE

For information on shared memory addresses, see page 13 – 12.

Procedure 2: PLS/PWM frequency settings in the shared memory

After the PLS/PWM settings have been set in the shared memory, the frequency of the output pulses should be specified.

A value between 1 Hz and 100 kHz should be specified, in units of 1 Hz.
When a value of 131.072 kHz or higher is specified, the output goes off (pulses are stopped).

When 0 Hz is set for the set value and the data is updated, pulse output stops.

	Address	
PLS0/PWM0 frequency setting	148h 149h	For PLS: K0 to K100000
PLS1/PWM1 frequency setting	14Ah 14Bh	For PLS: K0 to K100000
PLS2/PWM2 frequency setting	14Ch 14Dh	For PLS: K0 to K100000
PLS3/PWM3 frequency setting	14Eh 14Fh	For PLS: K0 to K100000

Notes

- **The shared memory should always be accessed in two−word units.**
- **The PLS/PWM setting should be set in the shared memory first, followed by the PLS/PWM frequency setting. Reversing the order will interfere with normal operation.**
- **If this is set to 0 Hz (K0), no pulses are output.**
- **To avoid malfunctions, make sure the values set do not exceed the rated values.**
- **The upper limit for error detection for the PLS frequency setting is 1048.575 kHz (1048.575 kHz = FFFFFh). If a value is set that exceeds this value, normal operation does not take place. For more detailed information, see page. 1 – 16.**

◆ REFERENCE

- **PLS/PWM flags are available at addresses 142h and 143h of the shared memory. Reading the statuses of the flags at these addresses enables monitoring of pulse output. For more information, see page 13 – 26.**
- **For information on shared memory addresses, see page 13 – 12.**

Procedure 3: PLS control signals

After the shared memory settings have been entered, control of the Enable, Start and Direction signals is necessary using the PLS control signal.

Enable signal

The Enable signal controls whether pulse output is valid or to be stopped.

on: Pulse output is valid.
off: Pulse output stops.

Start signal

The Start signal initiates pulse output and changes the output pulse frequency.

The frequency can also be changed by manipulating the timing of the “Comparison Matching” and “Data Update” parameters, under the “Pulse output settings”.
This signal is valid only when the Enable signal is on, and becomes invalid if the Enable signal goes off. Pulse output is enabled when both the Enable signal and the Start signal go on at the same time.

Direction signal

The Direction signal controls the direction of the pulse output.

off: Forward
on: Backward

Direction signal	Direction control output	Individual output
off (Forward)	Pulse output from PLSx A PLSx B off	Pulse output from PLSx A PLSx B off
on (Backward)	Pulse output from PLSx A PLSx B on	Pulse output from PLSx B PLSx A off

The table below shows the output allocations for the various control signals.

Table of control signal allocations

<table>
<tr><th rowspan="2">Output allocation</th><th colspan="3">Function</th></tr>
<tr><th>Pulse output CH</th><th colspan="2">Control content</th></tr>
<tr><td>Y20</td><td>PLS0</td><td rowspan="4">Direction control</td><td rowspan="4">When off: Forward For direction control output: PLSx B off
For individual output: Pulse output from PLSx A
When on: Backward For direction control output: PLSx B on
For individual output: Pulse output from PLSx B</td></tr>
<tr><td>Y21</td><td>PLS1</td></tr>
<tr><td>Y22</td><td>PLS2</td></tr>
<tr><td>Y23</td><td>PLS3</td></tr>
<tr><td>Y38</td><td>PLS0</td><td rowspan="4">Enable control</td><td rowspan="4">When off: Pulse output stops
When on: Pulse output is valid</td></tr>
<tr><td>Y39</td><td>PLS1</td></tr>
<tr><td>Y3A</td><td>PLS2</td></tr>
<tr><td>Y3B</td><td>PLS3</td></tr>
<tr><td>Y3C</td><td>PLS0</td><td rowspan="4">Start control</td><td rowspan="4">When first on: Pulse output begins
At leading edge (off → on): Output pulse frequency changes</td></tr>
<tr><td>Y3D</td><td>PLS1</td></tr>
<tr><td>Y3E</td><td>PLS2</td></tr>
<tr><td>Y3F</td><td>PLS3</td></tr>
</table>

Notes

- **The Direction signal can be changed during pulse output, but the timing in relation to the pulse output cannot be specified, so the signal should be changed when pulses have been stopped.**
- **Please be aware that, if the Enable signal is turned off during pulse output, the pulse output goes off at that point.**

10.1.3 Timing at Which Changes are Reflected in Output When Data is Changed

Timing at which data is changed

With the Pulse I/O Unit, the three modes described below are provided as the timing at which output frequency data is updated.

1. Data is updated at the rise of the PLS Start signal.
   In this mode, the frequency value to be changed is written to the shared memory ahead of time, and the data is updated at the point when the PLS Start signal goes from off to on.

2. Data is updated when the results of a comparison are output.
   In this mode, the frequency value to be changed is written to the shared memory ahead of time, and the data is updated at the point when the counter elapsed value matches the comparison value.

3. Data is updated when the data is refreshed.
   In this mode, the data is updated when the frequency value to be changed is written to the shared memory.

Timing at which changes are reflected in output

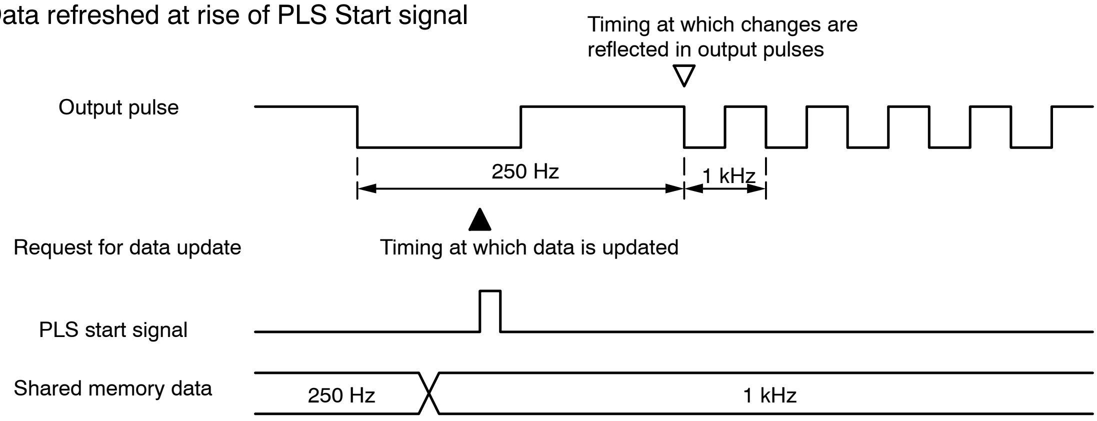
Frequency values updated at the timing described above are reflected at the next fall of the pulse being output.
For more detailed information, see the timing chart on the following page.

☞ **Note**

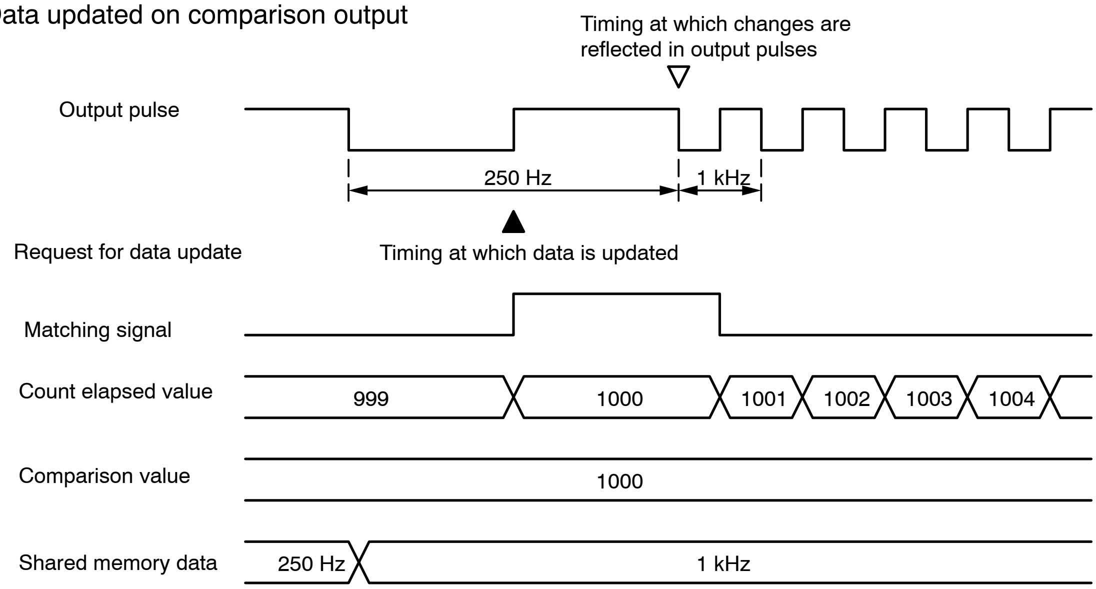
Data updated when the data was changed is reflected at the next fall of the pulse being output.
Please be aware that this means, if data was updated several times during one cycle, the most recent data changes will be reflected.

Timing chart

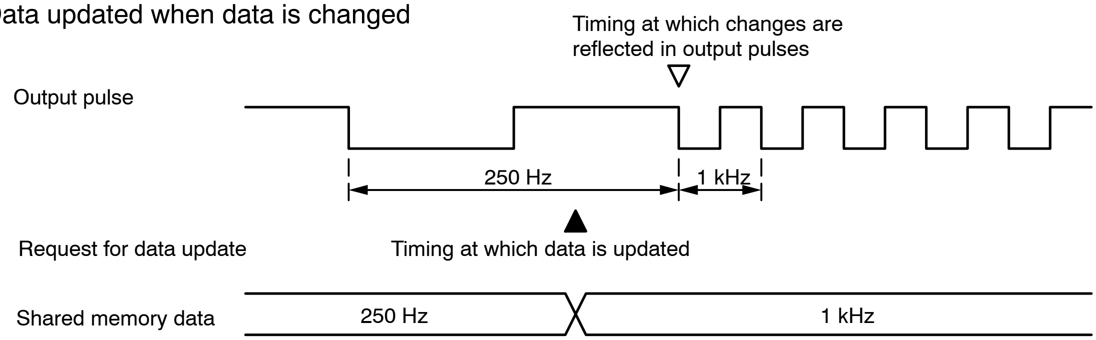
Data refreshed at rise of PLS Start signal



Data updated on comparison output

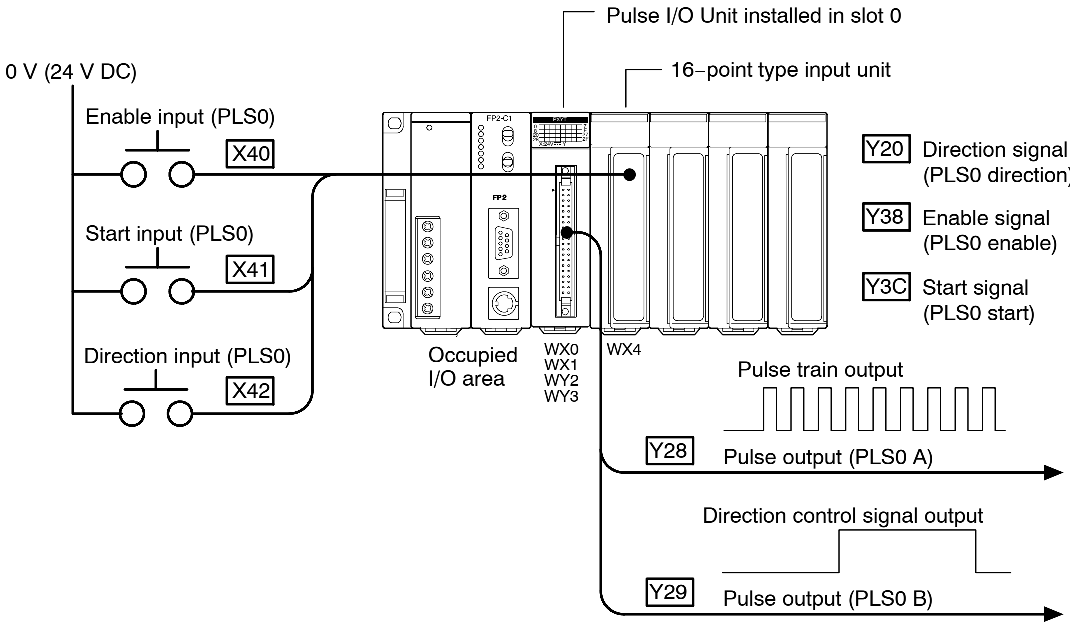


Data updated when data is changed



10.2 Using the Pulse Output Function

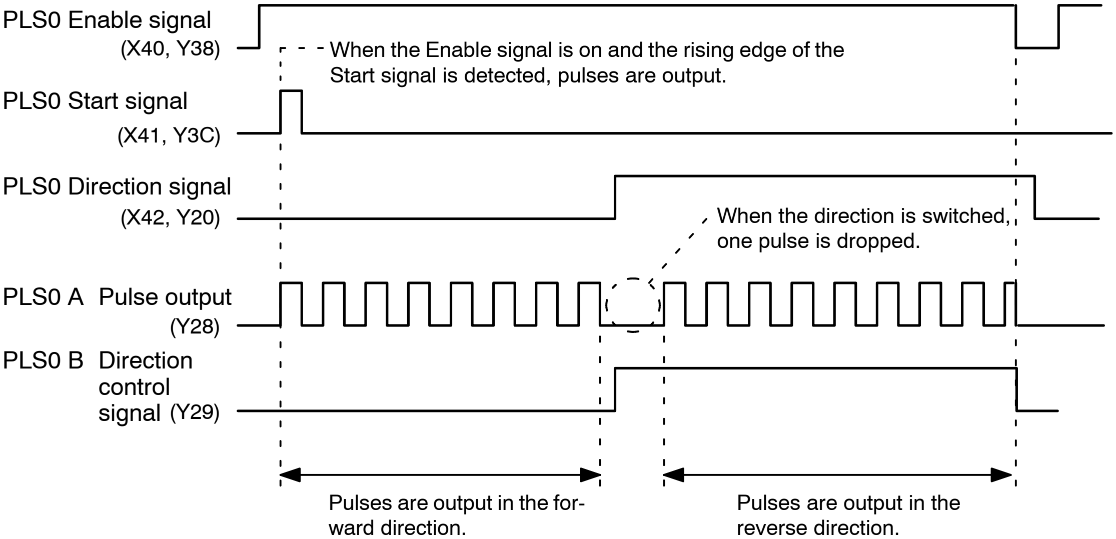
10.2.1 Overview



Pulses are output in the direction control mode. When the Enable input (X40) is turned on and the Start input goes on, pulses are output from Y28 and Y29 (PLS0). When the Direction input (X42) goes on, pulses are switched to the opposite direction.

10.2.2 Timing Chart

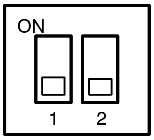
The following table shows the changes in pulse output in response to the input statuses of the various signals.



10.2.3 Setting the Mode Setting Switches

Mode A should be set if no interrupts are being used.

Mode A (SW1 → off, SW2 → off)



No interruption

When this setting is used, the interrupt function will not operate even if used.

The pulse output function can be used regardless of whether the interrupt function is set to “Used”or “Not Used”.

10.2.4 Shared Memory Settings

PLS/PWM setting

The PLS/PWM setting is used to specify the pulse output type.
In the example shown here, pulses are being output from Y28 and Y29 (PLS0) in the direction control mode, in which data is updated at the rise of the PLSx Start signal, so a value of “FFFFFFF4” should be written to addresses 140h and 141h of the shared memory.

Setting of shared memory addresses 140h and 141h

(bit)	32			16	15			0
Output number	Not used	Not used	Not used	Not used	PLS3	PLS2	PLS1	PLS0
Setting item	Not used	Not used	Not used	Not used	Type setting	Type setting	Type setting	Type setting
Set value	F	F	F	F	F	F	F	4
Function	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Data updated at Start signal (direction control)

PLS/PWM frequency setting

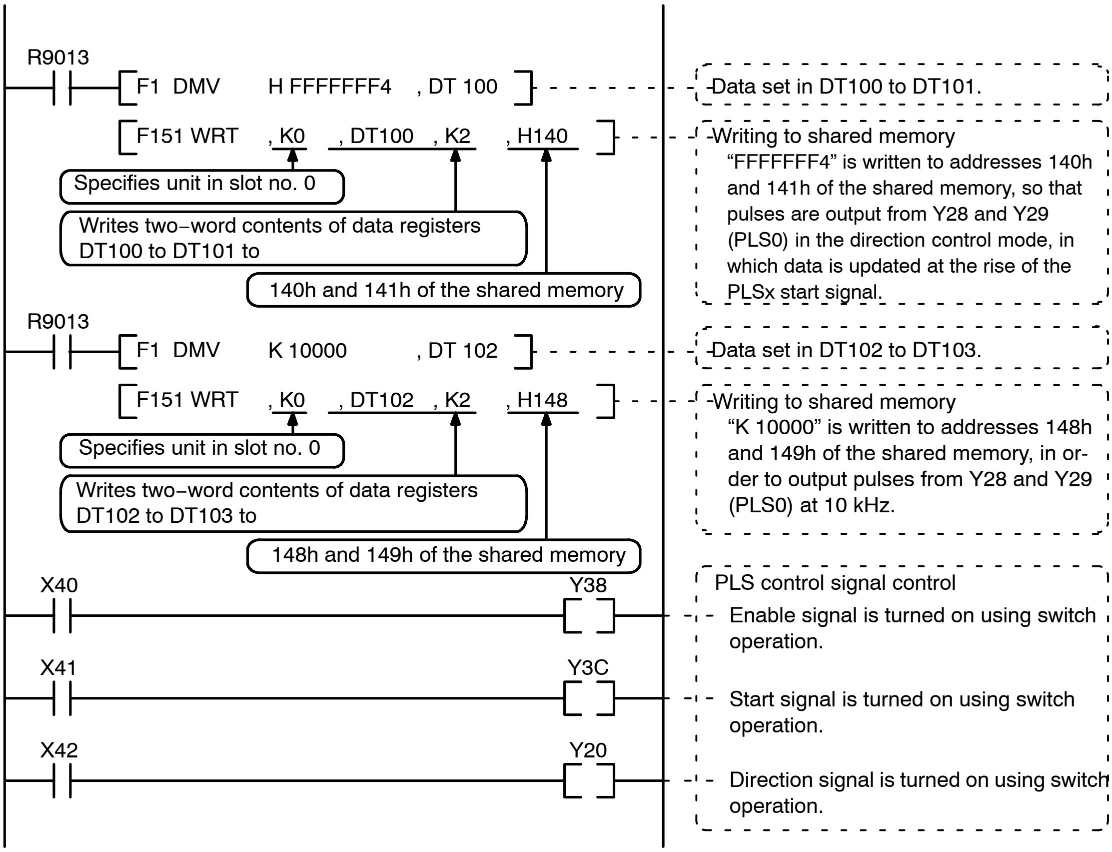
The PLS/PWM frequency setting is used to specify the frequency of the pulses.
In the example shown here, pulses are being output from Y28 and Y29 (PLS0) at 10 kHz, so a value of “K 10000 (H 2710)” should be written to addresses 148h and 149h of the shared memory.

Setting of shared memory addresses 148h and 149h

(bit)	32			16	15			0
Setting item	PLS0/PWM0 frequency setting							
Set value	0	0	0	0	2	7	1	0
Setting contents (Decimal)	K10000							

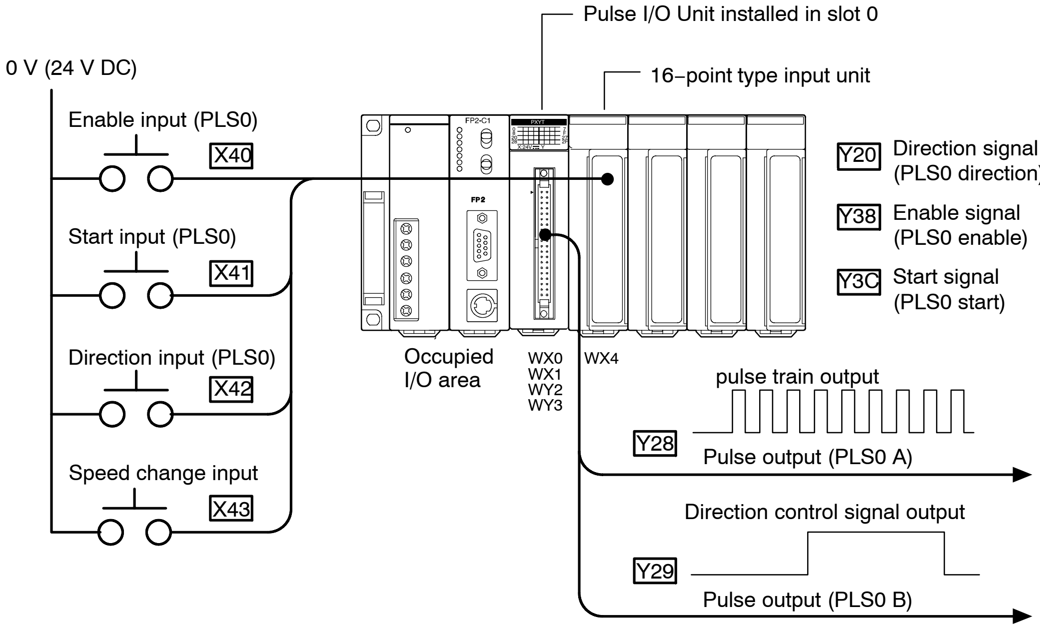
10.2.5 Sample Program

The settings relating to the pulse output function are entered in the shared memory, and then pushbutton operation is used to output pulses.



10.3 Changing the Frequency Using the Pulse Output Function

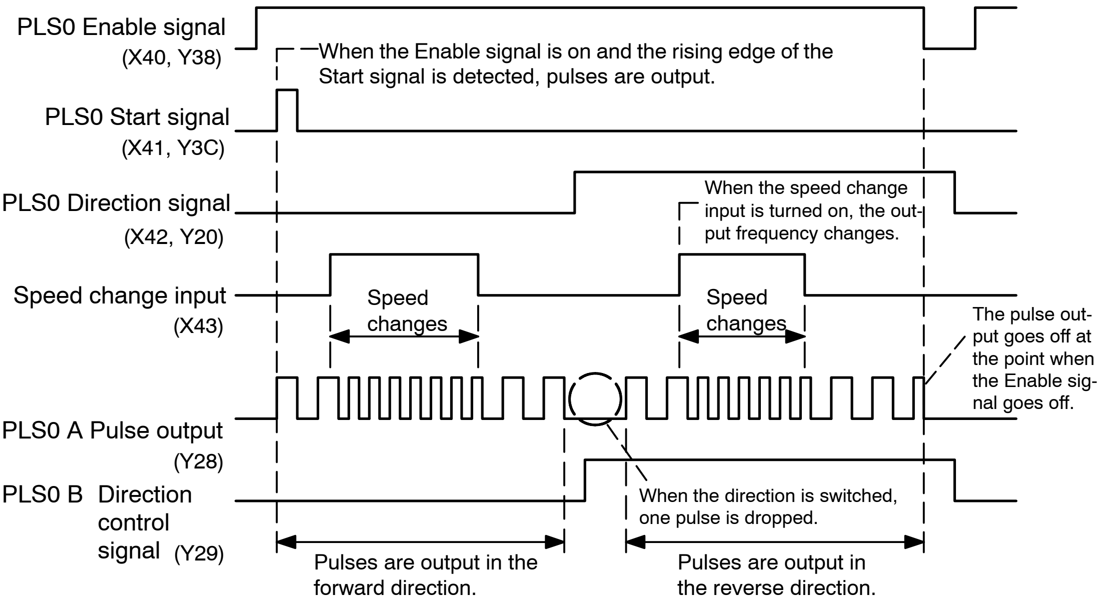
10.3.1 Overview



Pulses are output in the direction control mode. When the Enable input (X40) is turned on and the Start input goes on, pulses are output from Y28 and Y29 (PLS0). Also, when the direction input (X42) is turned on the pulses are switched to the reverse direction, and when the speed change input (X43) is turned on, the frequency of the output pulses is changed.

10.3.2 Timing Chart

The following table shows the changes in pulse output in response to the input statuses of the various signals.



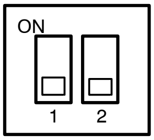
Note

If the number of pulses is extremely close to the point at which the frequency changes, there may be times when the frequency cannot be changed because of delays in internal processing (scan time).
As a general guide, the system will run at the prescribed values as long as the pulse output time is larger than the time required for two PLC scans. For example, if 10 pulses are output at 1 kHz, the pulse output time will be 10 ms, so the PLC scan time should be 5 ms or less.

10.3.3 Setting the Mode Setting Switches

Mode A should be set if no interrupts are being used.

Mode A (SW1 → off, SW2 → off)



No interruption

When this setting is used, the interrupt function will not operate even if used.

The pulse output function can be used regardless of whether the interrupt function is set to “Used” or “Not Used”.

10.3.4 Shared Memory Settings

PLS/PWM setting

The PLS/PWM setting is used to specify the pulse output type.
In the example shown here, pulses are output from Y28 and Y29 (PLS0) in the direction control mode in which the frequency (speed) is changed at the rise of the PLSx Start signal or when the data is updated, so a value of “FFFFFFF8” should be written to addresses 140h and 141h of the shared memory.

Setting of shared memory addresses 140h and 141h

(bit)	32			16	15			0
Output number	Not used	Not used	Not used	Not used	PLS3	PLS2	PLS1	PLS0
Setting item	Not used	Not used	Not used	Not used	Type setting	Type setting	Type setting	Type setting
Set value	F	F	F	F	F	F	F	8
Output type	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Updated at Start signal or when data is changed (direction control)

PLS/PWM frequency setting

The PLS/PWM frequency setting is used to specify the frequency of the pulses.
In the example shown here, pulses are being output from Y28 and Y29 (PLS0) at 10 kHz, so a value of “K 10000 (H 2710)” should be written to addresses 148h and 149h of the shared memory. This data is rewritten to “K 20000 (H 4E20)” at the timing at which the speed change input (X43) goes on.

Setting of shared memory addresses 148h and 149h

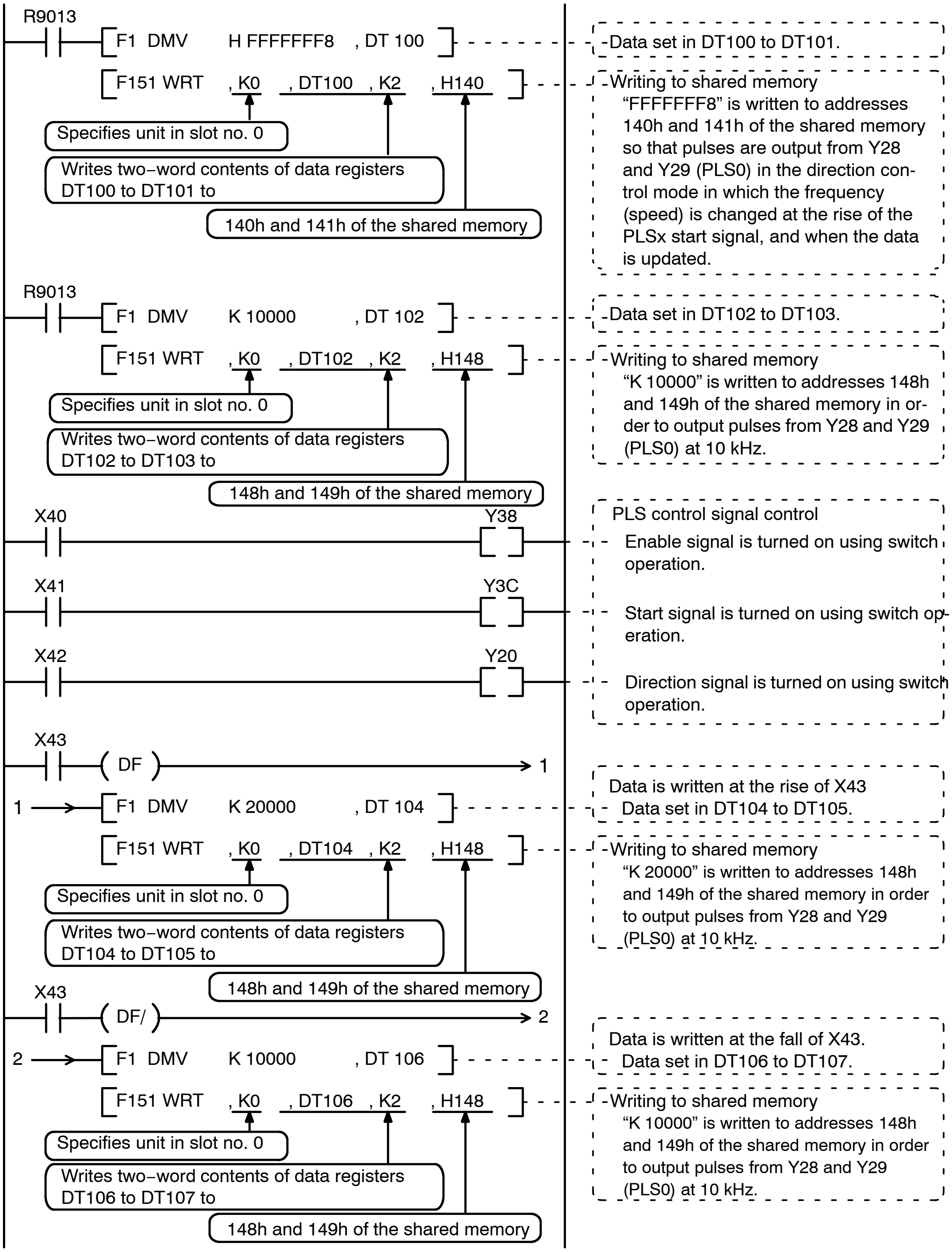
(bit)	32			16	15			0
Setting item	PLS0/PWM0 frequency setting							
Set value	0	0	0	0	2	7	1	0
Setting contents (Decimal)	K10000							

When X43 is on

(bit)	32			16	15			0
Setting item	PLS0/PWM0 frequency setting							
Set value	0	0	0	0	4	E	2	0
Setting contents (Decimal)	K20000							

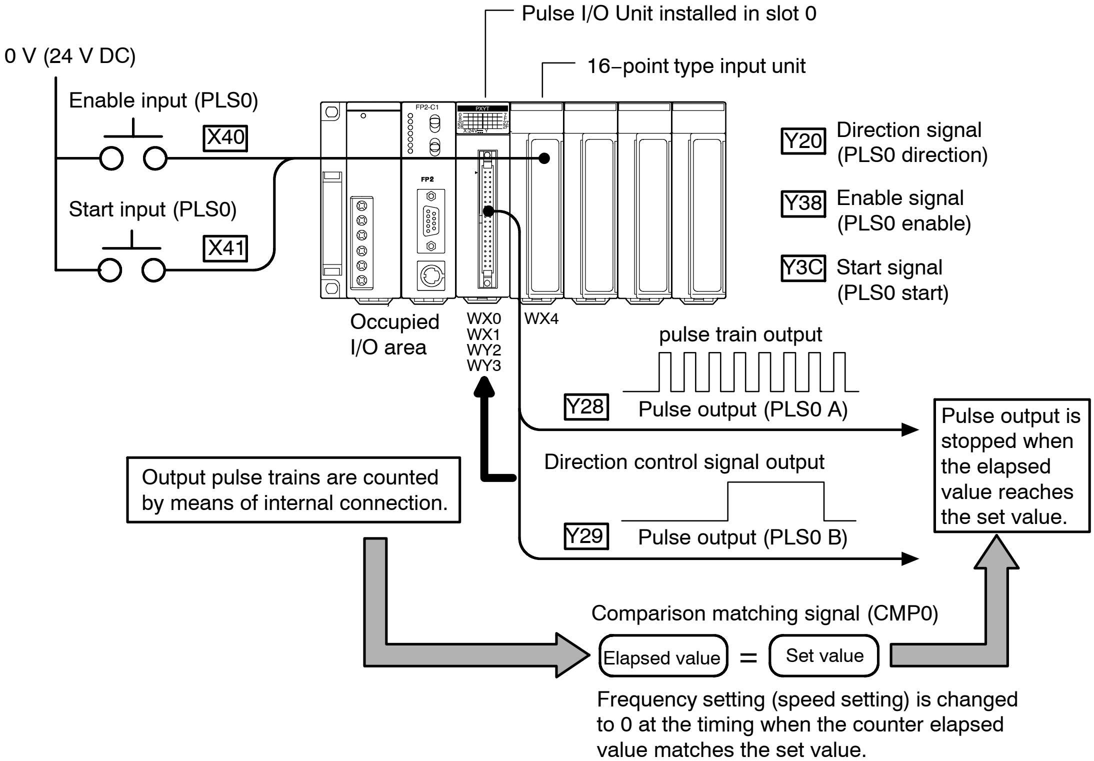
10.3.5 Sample Program

The settings relating to the pulse output function are entered in the shared memory, and then pushbutton operation is used to output pulses.



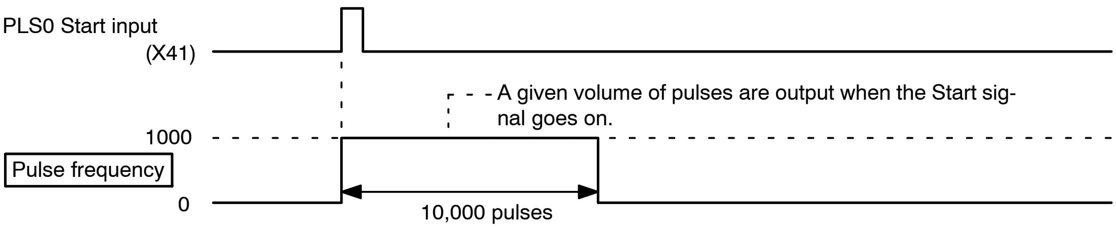
10.4 Specified Pulse Output Using the Pulse Output Function

10.4.1 Overview



Pulses are output in the direction control mode. When the Enable input for X40 is turned on and the Start input goes on, pulses are output from Y28 and Y29 (PLS0). The output pulses are fed back to the high−speed counter in the unit, and when a previously specified value is reached, pulse output stops.

Pulse output diagram



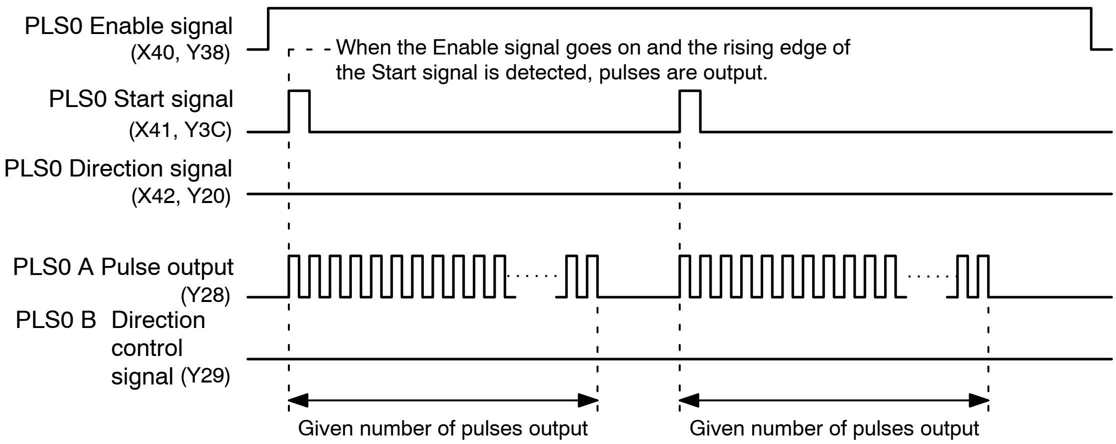
10,000 pulses equivalent to a 1 kHz pulse are output when the Start signal is input.

Notes

- **If the number of pulses output is extremely low, the pulse output may not stop when the given value is reached in some cases, because of delays in internal processing (scan time). As a general guide, the system will run at the prescribed values as long as the pulse output time is larger than the time required for two PLC scans. For example, if 10 pulses are output at 1 kHz, the pulse output time will be 10 ms, so the PLC scan time should be 5 ms or less.**
- **When the pulse output is internally connected to the counter, the counter input mode is automatically set to match the pulse output. Please be aware that this causes the counter input mode set in advance to be ignored.**
- **When the pulse output is internally connected to the counter, the channels that correspond to the counter and the pulse output are fixed.**

10.4.2 Timing Chart

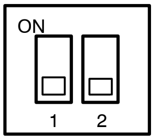
The following table shows the changes in pulse output in response to the input statuses of the various signals.



10.4.3 Setting the Mode Setting Switches

Mode A should be set if no interrupts are being used.

Mode A (SW1 → off, SW2 → off)



No interruption

When this setting is used, the interrupt function will not operate even if used.

The pulse output function can be used regardless of whether the interrupt function is set to “Used” or “Not Used”.

10.4.4 Shared Memory Settings

In the example shown here, the pulse output settings, the settings for the counter that counts the output pulses, and the settings relating to the comparison matching are set in the shared memory.

Counter Setting

This sets the operation modes for the various counter channels.
In this example, the counter function is being used in the direction control mode, and the output pulses are being counted by means of an internal connection, so a value of “FFFFFF02” should be written to addresses 100h and 101h of the shared memory.

Setting of shared memory addresses 100h and 101h

(bit)	32			16	15			0
External output	X7	X6	X5	X4	X3	X2	X1	X0
Counter number	CH3		CH2		CH1		CH0	
Setting item	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting
Set value	F	F	F	F	F	F	0	2
Setting contents	Not used	Not used	Not used	Not used	Not used	Not used	Direction control	Internal connection

Setting the Comparison Output set value

Here, the comparison output set value, which is compared to the counter elapsed value, is set.
In the example shown here, the value is set so that CMP0 is output when the counter elapsed value reaches “10000”. To do this, write a value of “K10000 (H2710)” to addresses 120h and 121h of the shared memory.

Setting of shared memory addresses 120h and 121h

(bit)	32			16	15			0
Setting item	Comparison output set value (for CMP0)							
Set value	0	0	0	0	2	7	1	0
Setting contents (Decimal)	K10000							

Comparison Output Setting

The channel number and output logic for the counter used in the comparison output function are selected.
In the example shown here, the value of “FFFFFFF0” should be written to addresses 104h and 105h of the shared memory, so that the elapsed value of the CH0 counter will be compared with the comparison output set value, and the result output to CMP0.

Setting of shared memory addresses 104h and 105h

(bit)	32			16	15			0
Comparison input	CMP7	CMP6	CMP5	CMP4	CMP3	CMP2	CMP1	CMP0
Set value	F	F	F	F	F	F	F	0
Comparison output function	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CH0 comparison*

* In the example shown here, the output logic from the CMP0 comparison output is set to go on if the elapsed value is smaller than the set value. To set this so that the output goes on if the elapsed value is larger than or equal to the set value, “FFFFFFF4” should be written to addresses 104h and 105h of the shared memory.

PLS/PWM setting

The PLS/PWM setting is used to specify the Pulse output type.
In the example shown here, pulses are output from Y28 and Y29 (PLS0) in the direction control mode in which the frequency (speed) is changed at the rise of the PLSx Start signal or when the comparison is output, so a value of “FFFFFFF6” should be written to addresses 140h and 141h of the shared memory.

Setting of shared memory addresses 140h and 141h

(bit)	32			16	15			0
Output number	Not used	Not used	Not used	Not used	PLS3	PLS2	PLS1	PLS0
Setting item	Not used	Not used	Not used	Not used	Type setting	Type setting	Type setting	Type setting
Set value	F	F	F	F	F	F	F	6
Setting contents	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Data updated at Start signal or on comparison output

PLS/PWM frequency setting

The PLS/PWM frequency setting is used to specify the frequency of the pulses.
In the example shown here, pulses are being output from Y28 and Y29 (PLS0) at 10 kHz, so a value of “K 1000 (H 3E8)” should be written to addresses 148h and 149h of the shared memory. To prepare to stop the pulses when the comparison is output, “K 0 (H 0)” should be written after the Start signal has been input and the pulses have been output.

Setting of shared memory addresses 148h and 149h

Before pulses start

(bit)	32			16	15			0
Setting item	PLS0/PWM0 frequency setting							
Set value	0	0	0	0	0	3	E	8
Setting contents (Decimal)	K1000							

After pulses start

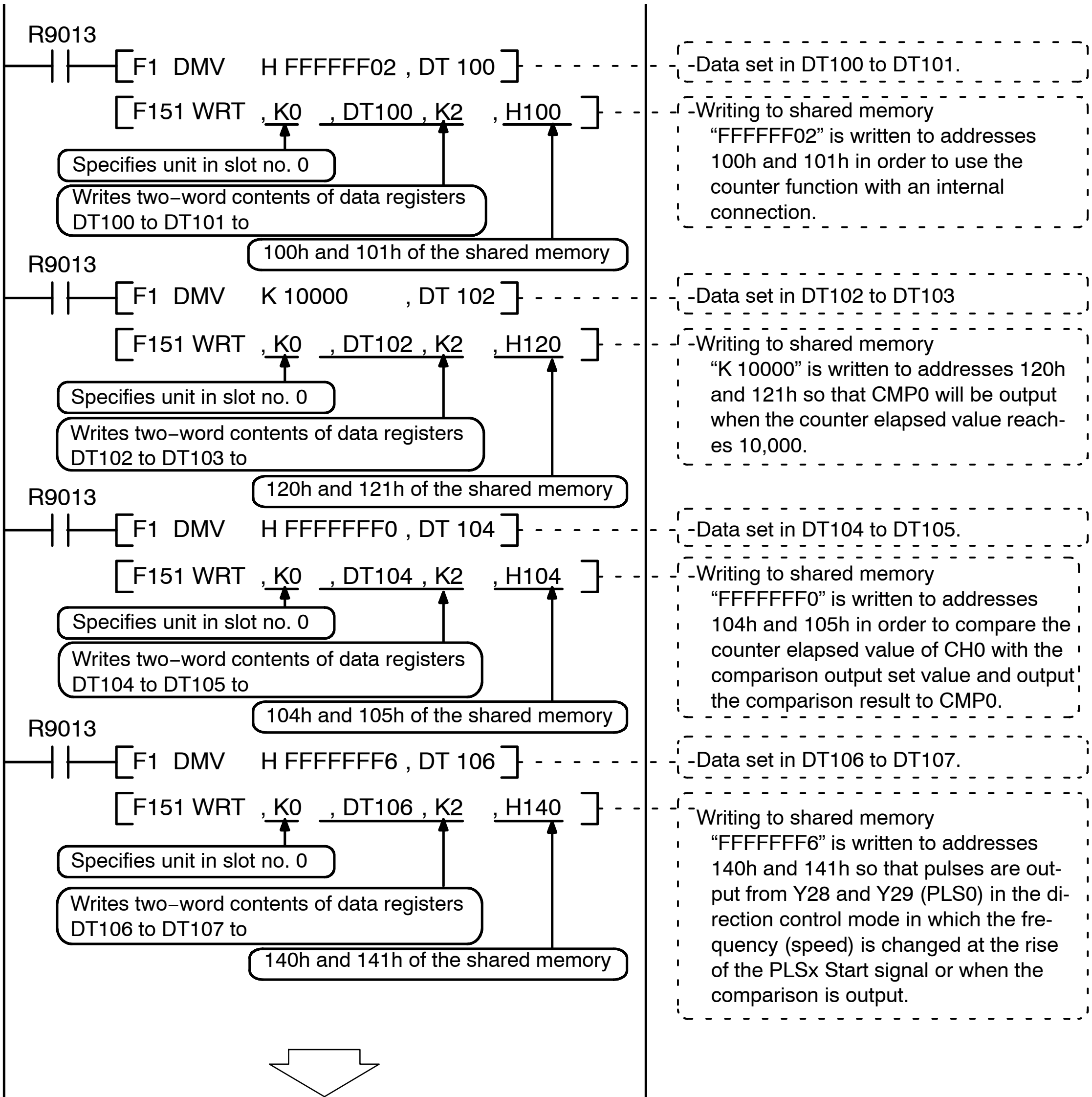
(bit)	32			16	15			0
Setting item	PLS0/PWM0 frequency setting							
Set value	0	0	0	0	0	0	0	0
Setting contents (Decimal)	K0							

☞ **Note**

When the pulse output is internally connected to the counter and the pulse frequency (speed) is being changed at the timing at which the counter elapsed value matches the set value, the same channel should be specified for the CMP output for both PLSx and PWMx.

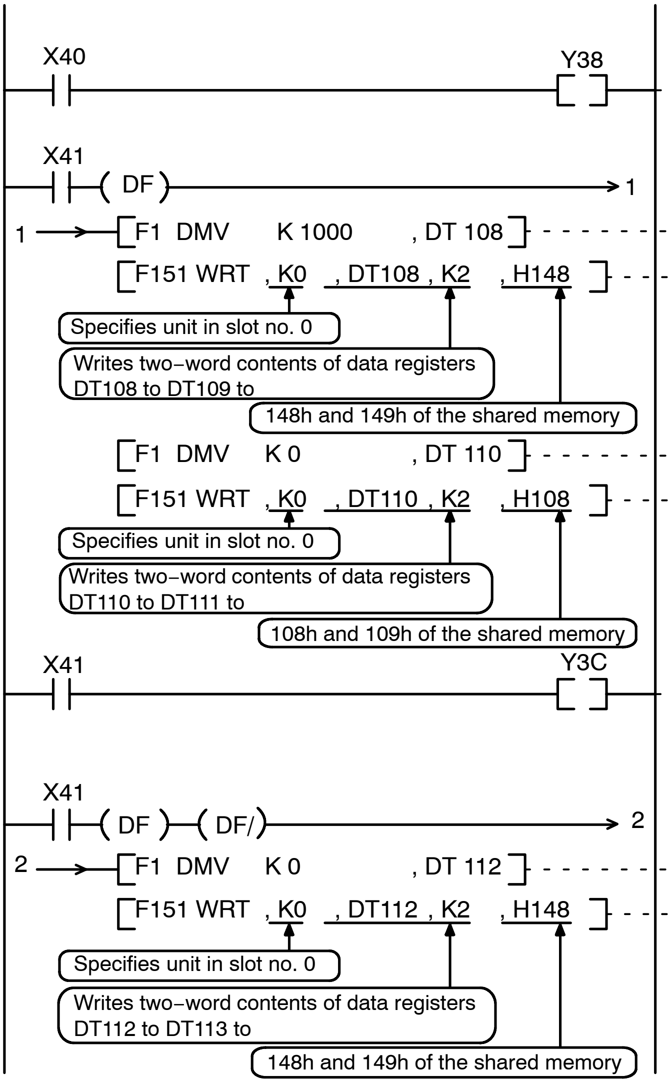
10.4.5 Sample Program

These programs are for setting the pulse output fucntion, counter function and comparison function in the shared memory, and for operating the pushbuttons.



next page

10.4 Specified Pulse Output Using the Pulse Output Function



PLS control signal control
Enable signal is turned on using switch operation.

Speed is set using the Start signal timing.

-Data set in DT108 to DT109

-Writing to shared memory
"K 1000" is written to addresses 148h and 149h of the shared memory in order to output pulses from Y28 and Y29 (PLS0) at 1k Hz.

-Data set in DT110 to DT111.

-Writing to shared memory
"0" is written to addresses 108h and 109h to reset the counter elapsed value.

PLS control signal control
Start signal is turned on using switch operation.

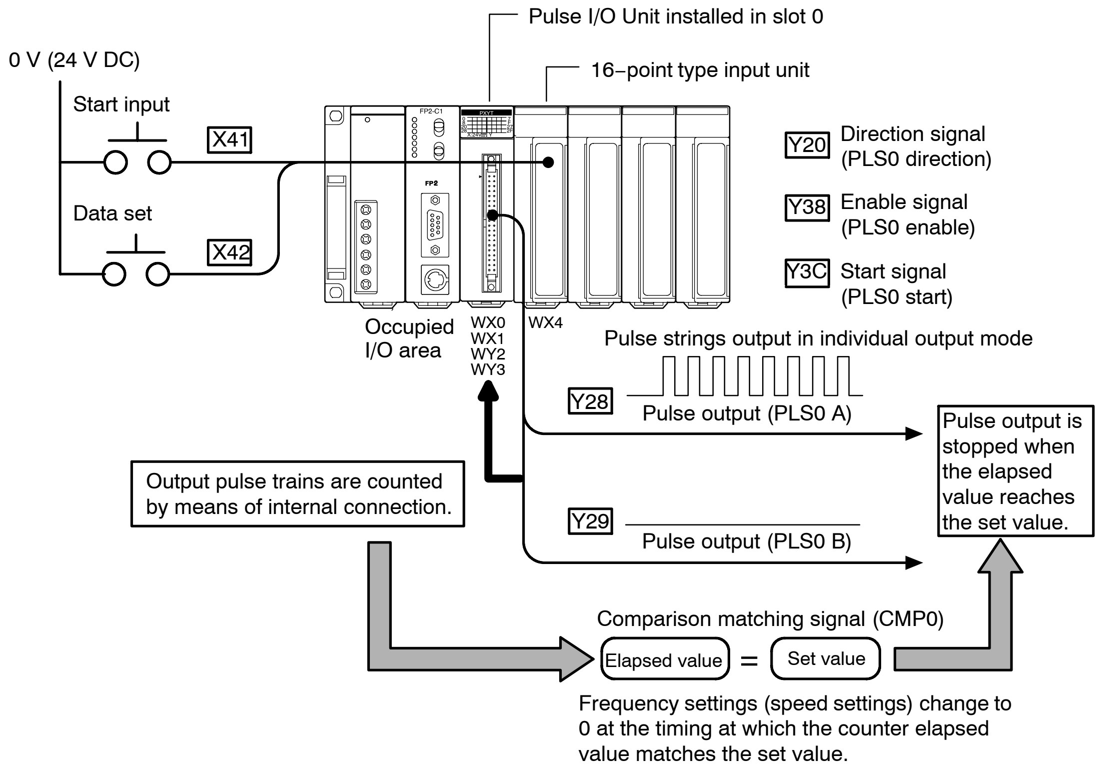
This stops pulses (sets the speed to 0) one scan delay after the Start signal has been issued.

-Data set in DT112 to DT113.

-Writing to shared memory
"K 0" is written to addresses 148h and 149h to stop the pulse output (0k Hz) from Y28 and Y29 (PLS0).

10.5 Determining the Absolute Value Position Using the Pulse Output Function

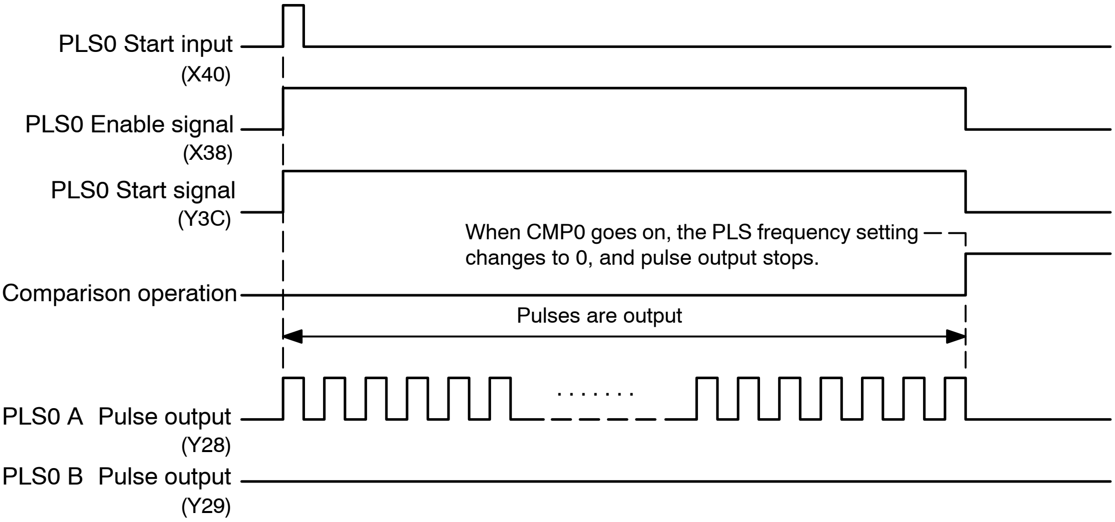
10.5.1 Overview



Pulses are output in the individual output mode. The data set for X42 is turned on and a target value is set for DT500.
Subsequently, when the X40 Start input is turned on, the prescribed pulses are output from Y28 and Y29 (PLS0), moving in the direction of the target value. Pulses are output in the absolute value mode, in which the forward and reverse directions are automatically switched in response to the current value and the target value.

10.5.2 Timing Chart

The following table shows the changes in pulse output in response to the input statuses of the various signals.



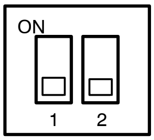
Notes

- **When the pulse output is internally connected to the counter, the counter input mode is automatically set to a mode that matches the pulse output. Please be aware that, for this reason, the counter input mode specified ahead of time will be ignored.**
- **With the internal connection to the pulse output counter, the channels corresponding to the counter and the pulse output are fixed.**

10.5.3 Setting the Mode Setting Switches

Mode A should be set if no interrupts are being used.

Mode A (SW1 → off, SW2 → off)



No interruption

When this setting is used, the interrupt function will not operate even if used.

The pulse output function can be used regardless of whether the interrupt function is set to “Used” or “Not Used”.

10.5.4 Shared Memory Settings

In the example shown here, the pulse output settings, the settings for the counter that counts the output pulses, and the settings relating to the comparison matching are set in the shared memory.

Counter Setting

This sets the operation modes for the various counter channels.
In this example, the counter function is being used in the direction control mode, and the output pulses are being counted by means of an internal connection, so a value of “FFFFFF02” should be written to addresses 100h and 101h of the shared memory.

Setting of shared memory addresses 100h and 101h

(bit)	32			16	15			0
External output	X7	X6	X5	X4	X3	X2	X1	X0
Counter number	CH3		CH2		CH1		CH0	
Setting item	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting
Set value	F	F	F	F	F	F	0	2
Setting contents	Not used	Not used	Not used	Not used	Not used	Not used	Direction control	Internal connection

Comparison Output Setting

The channel number and output logic for the counter used in the comparison output function are selected.
In the example shown here, the value of “FFFFFFF4” should be written to addresses 104h and 105h of the shared memory, so that the elapsed value of the CH0 counter will be compared with the comparison output set value, and the result output to CMP0.

Setting of shared memory addresses 104h and 105h

(bit)	32			16	15			0
Comparison input	CMP7	CMP6	CMP5	CMP4	CMP3	CMP2	CMP1	CMP0
Set value	F	F	F	F	F	F	F	4
Setting contents	Not used	Not used	Not used	Not used	Not used	Not used	Not used	CH0 comparison*

* In the example shown here, the output logic of the comparison output for CMP0 is set to go on if the elapsed value is larger than or equal to the set value, but to set this so that the output logic goes on if the elapsed value is smaller than the set value, “FFFFFFF0” should be written to addresses 104h and 105h of the shared memory.

Setting the Comparison Output set value

Here, the comparison output set value, which is compared to the counter elapsed value, is set.
In the example shown here, the settings have been entered so that DT500 is written to K500 when the data is set, and CMP0 is output when the counter elapsed value reaches 500, so “K500 (H1F4)” is written to addresses 120h and 121h of the shared memory.

Setting of shared memory addresses 120h and 121h

(bit)	32			16	15			0
Setting item	Comparison output set value (for CMP0)							
Set value (HEX)	0	0	0	0	0	1	F	4
Setting contents (Decimal)	K500							

PLS/PWM setting

The PLS/PWM setting is used to specify the pulse output type.
In the example shown here, pulses are output from Y28 and Y29 (PLS0) in the individual output mode in which the frequency (speed) is changed at the rise of the PLSx Start signal, or when the comparison is output, so a value of “FFFFFFF7” should be written to addresses 140h and 141h of the shared memory.

Setting of shared memory addresses 140h and 141h

(bit)	32			16	15			0
Output number	Not used	Not used	Not used	Not used	PLS3	PLS2	PLS1	PLS0
Setting item	Not used	Not used	Not used	Not used	Type setting	Type setting	Type setting	Type setting
Set value	F	F	F	F	F	F	F	7
Setting contents (Function)	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Data updated at Start signal or on comparison output

PLS/PWM frequency setting

The PLS/PWM frequency setting is used to specify the frequency of the pulses.
In the example shown here, pulses are being output from Y28 and Y29 (PLS0) at 1 kHz, so a value of “K 1000 (H 3E8)” should be written to addresses 148h and 149h of the shared memory. For comparison output, this value is substituted for “K0 (H0)” when the R1 relay falls, in preparation for stopping the pulse frequency (speed).

Setting of shared memory addresses 148h and 149h

On pulse output

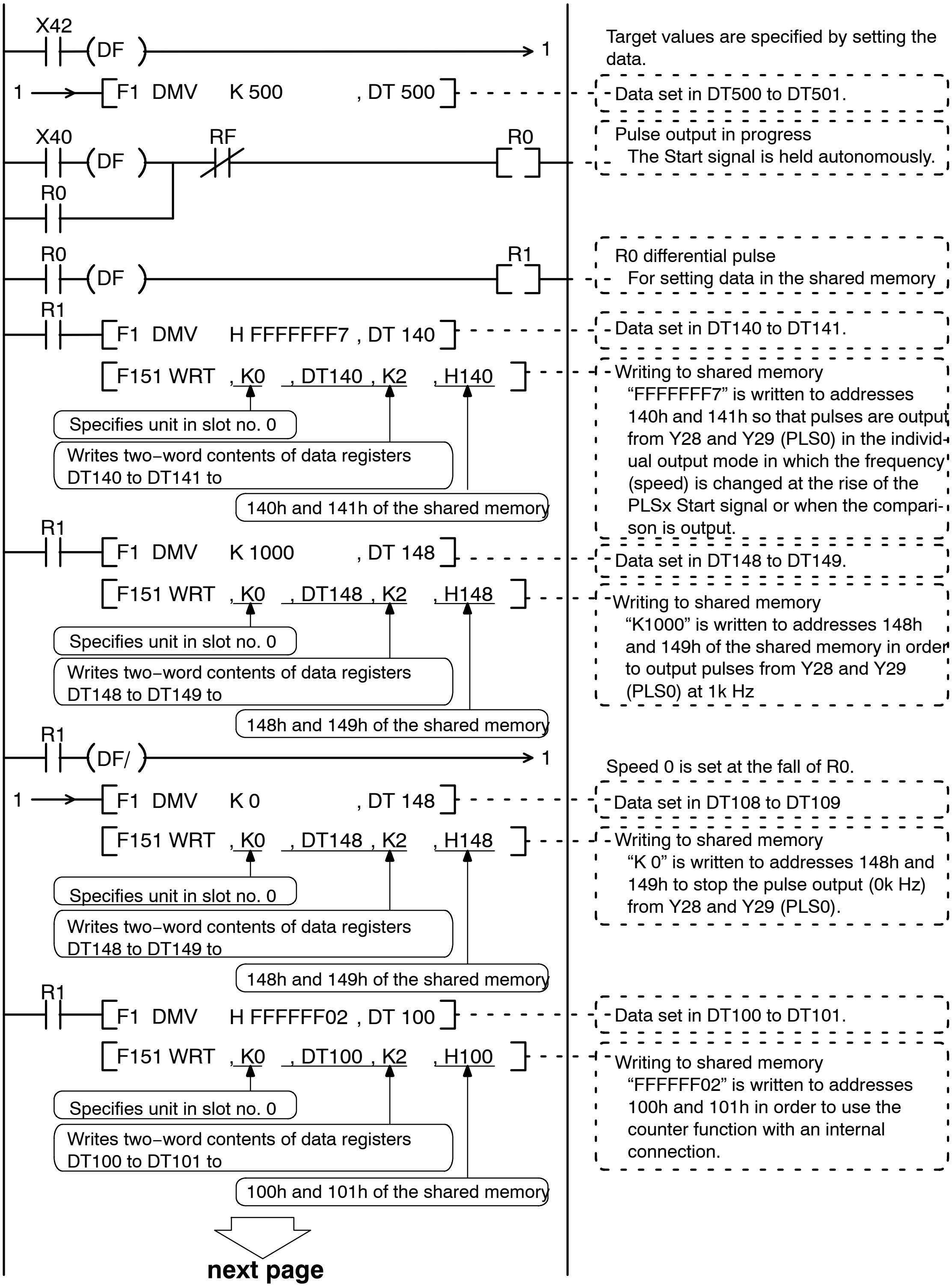
(bit)	32			16	15			0
Setting item	PLS0/PWM0 frequency setting							
Set value (HEX)	0	0	0	0	0	3	E	8
Setting contents (Decimal)	K1000							

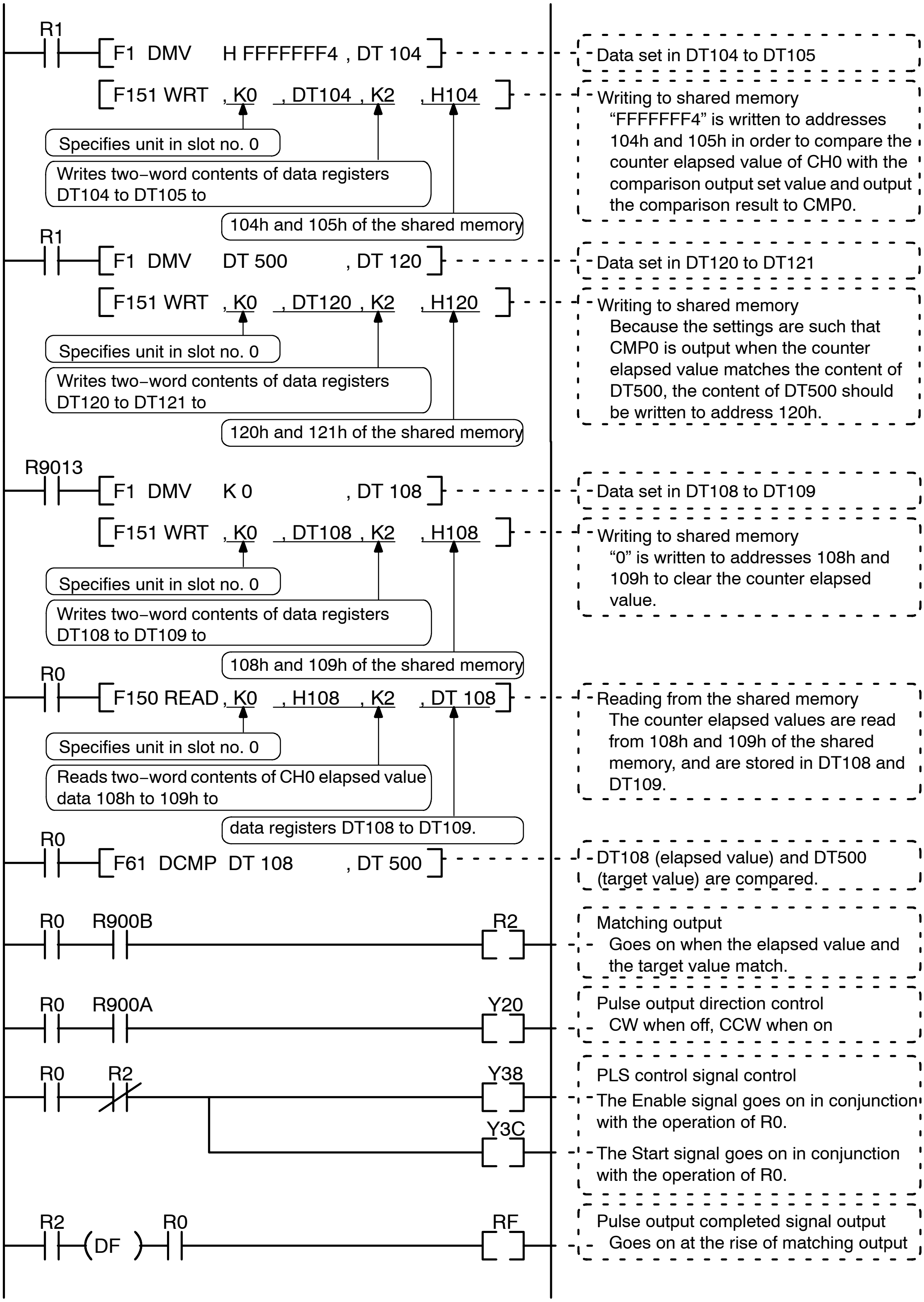
When stopped

(bit)	32			16	15			0
Setting item	PLS0/PWM0 frequency setting							
Set value (HEX)	0	0	0	0	0	0	0	0
Setting contents (Decimal)	K0							

10.5.5 Sample Program

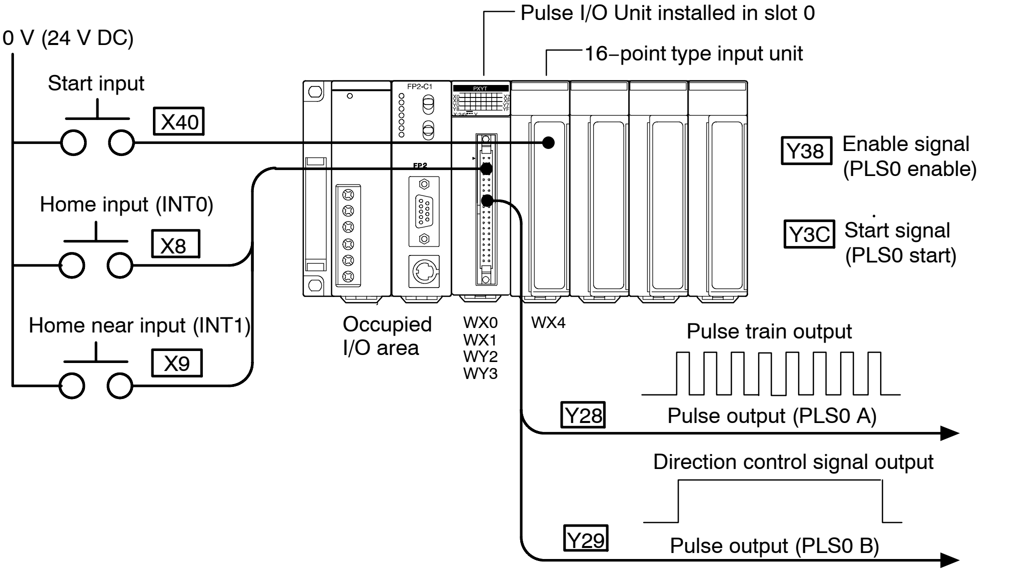
These programs are for setting the pulse output fucntion, counter function and comparison function in the shared memory, and for operating the pushbuttons.

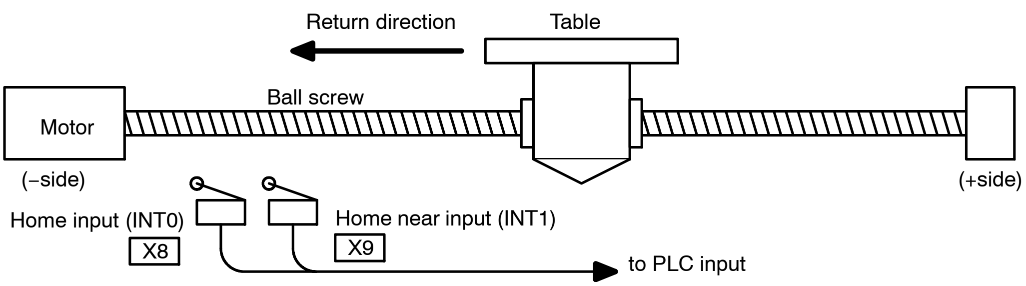



R1
F1 DMV H FFFFFFF4 , DT 104
Data set in DT104 to DT105
F151 WRT , K0 , DT104 , K2 , H104
Specifies unit in slot no. 0
Writes two−word contents of data registers DT104 to DT105 to
104h and 105h of the shared memory
Writing to shared memory
"FFFFFFF4" is written to addresses 104h and 105h in order to compare the counter elapsed value of CH0 with the comparison output set value and output the comparison result to CMP0.
R1
F1 DMV DT 500 , DT 120
Data set in DT120 to DT121
F151 WRT , K0 , DT120 , K2 , H120
Specifies unit in slot no. 0
Writes two−word contents of data registers DT120 to DT121 to
120h and 121h of the shared memory
Writing to shared memory
Because the settings are such that CMP0 is output when the counter elapsed value matches the content of DT500, the content of DT500 should be written to address 120h.
R9013
F1 DMV K 0 , DT 108
Data set in DT108 to DT109
F151 WRT , K0 , DT108 , K2 , H108
Specifies unit in slot no. 0
Writes two−word contents of data registers DT108 to DT109 to
108h and 109h of the shared memory
Writing to shared memory
"0" is written to addresses 108h and 109h to clear the counter elapsed value.
R0
F150 READ , K0 , H108 , K2 , DT 108
Specifies unit in slot no. 0
Reads two−word contents of CH0 elapsed value data 108h to 109h to
data registers DT108 to DT109.
Reading from the shared memory
The counter elapsed values are read from 108h and 109h of the shared memory, and are stored in DT108 and DT109.
R0
F61 DCMP DT 108 , DT 500
DT108 (elapsed value) and DT500 (target value) are compared.
R0 R900B R2
Matching output
Goes on when the elapsed value and the target value match.
R0 R900A Y20
Pulse output direction control
CW when off, CCW when on
R0 R2 Y38
Y3C
PLS control signal control
The Enable signal goes on in conjunction with the operation of R0.
The Start signal goes on in conjunction with the operation of R0.
R2 DF R0 RF
Pulse output completed signal output
Goes on at the rise of matching output

10.6 Home Return Using the Pulse Output Function

10.6.1 Overview

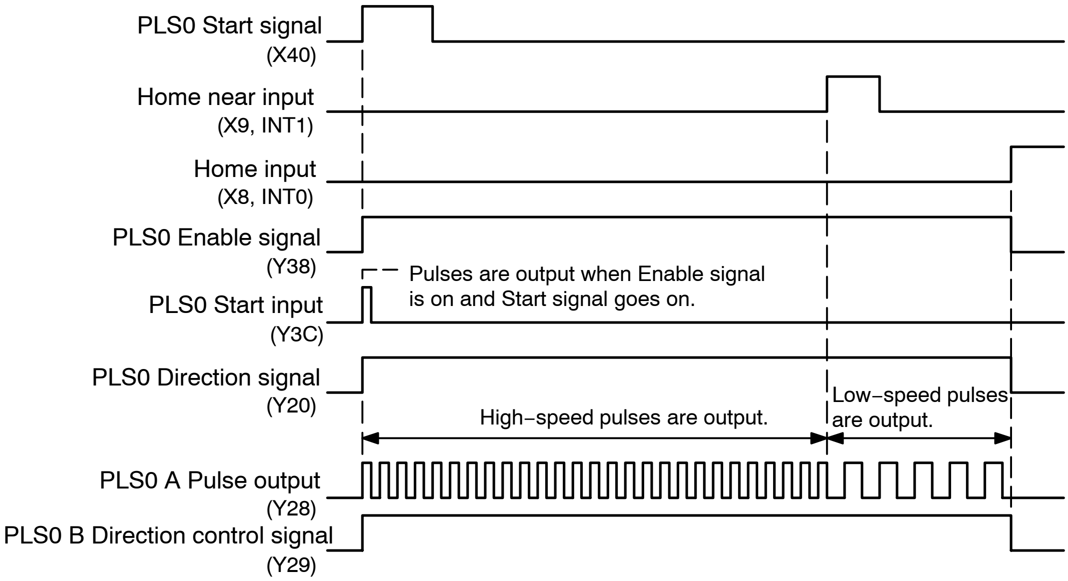




Pulses are output in the individual output mode. When the start input of X40 is turned on, pulses are output from Y28 and Y29 (PLS0). When X9 (INT1) is input, pulse output decelerates, and when X8 (INT0) is input, pulse output stops.

10.6.2 Timing Chart

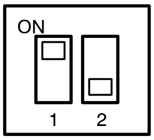
The following table shows the changes in pulse output in response to the input statuses of the various signals.



10.6.3 Setting the Mode Setting Switches

Set the mode setting switches to Mode B, so that all eight interrupts from INT0 to INT7 can be used.

Mode B (SW1 → on, SW2 → off)



With interruption (interrupt points:8)

Up to eight interrrupts can be used for each unit (INT0 to INT7).

When this mode is specified, eight interrupt points (INT0 to INT7) are automatically defined for the unit, regardless of whether or not the interrupt function is used.

10.6.4 Shared Memory Settings

In the example shown here, settings concerning interrupts used to slow and stop the output pulses are entered in the shared memory, along with settings concerning the pulse output.

Interrupt Setting

If the interrupt function is being used, settings must be entered in the shared memory, in addtion to setting the mode setting switches on the side panel of the main unit.

In the example shown here, interrupt signals are generated at the rise of the X8 and X9 external input (when the input goes from off to on), so “FFFFFF22” is written to addresses 138h and 139h of the shared memory.

Setting of shared memory addresses 138h and 139h

(bit)	32			16	15			0
External output	XF	XE	XD	XC	XB	XA	X9	X8
Interrupt number	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
Set value	F	F	F	F	F	F	2	2
Interrupt setting	Not used	Not used	Not used	Not used	Not used	Not used	off ! on	off ! on

PLS/PWM setting

The pulse output configuration is specified with the PLS/PWM setting.
In the example shown here, pulses are output from Y28 and Y29 (PLS0) in the individual output mode, in which the frequency (speed) is changed at the rise of the PLSx Start signal, or when the data is updated, so “FFFFFFF9” should be written to addresses 140h and 141h of the shared memory.

Setting of shared memory addresses 140h and 141h

(bit)	32			16	15			0
Output number	Not used	Not used	Not used	Not used	PLS3	PLS2	PLS1	PLS0
Setting item	Not used	Not used	Not used	Not used	Type setting	Type setting	Type setting	Type setting
Set value	F	F	F	F	F	F	F	9
Output type	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Updated at Start signal or when data is changed (individual output)

PLS/PWM frequency setting

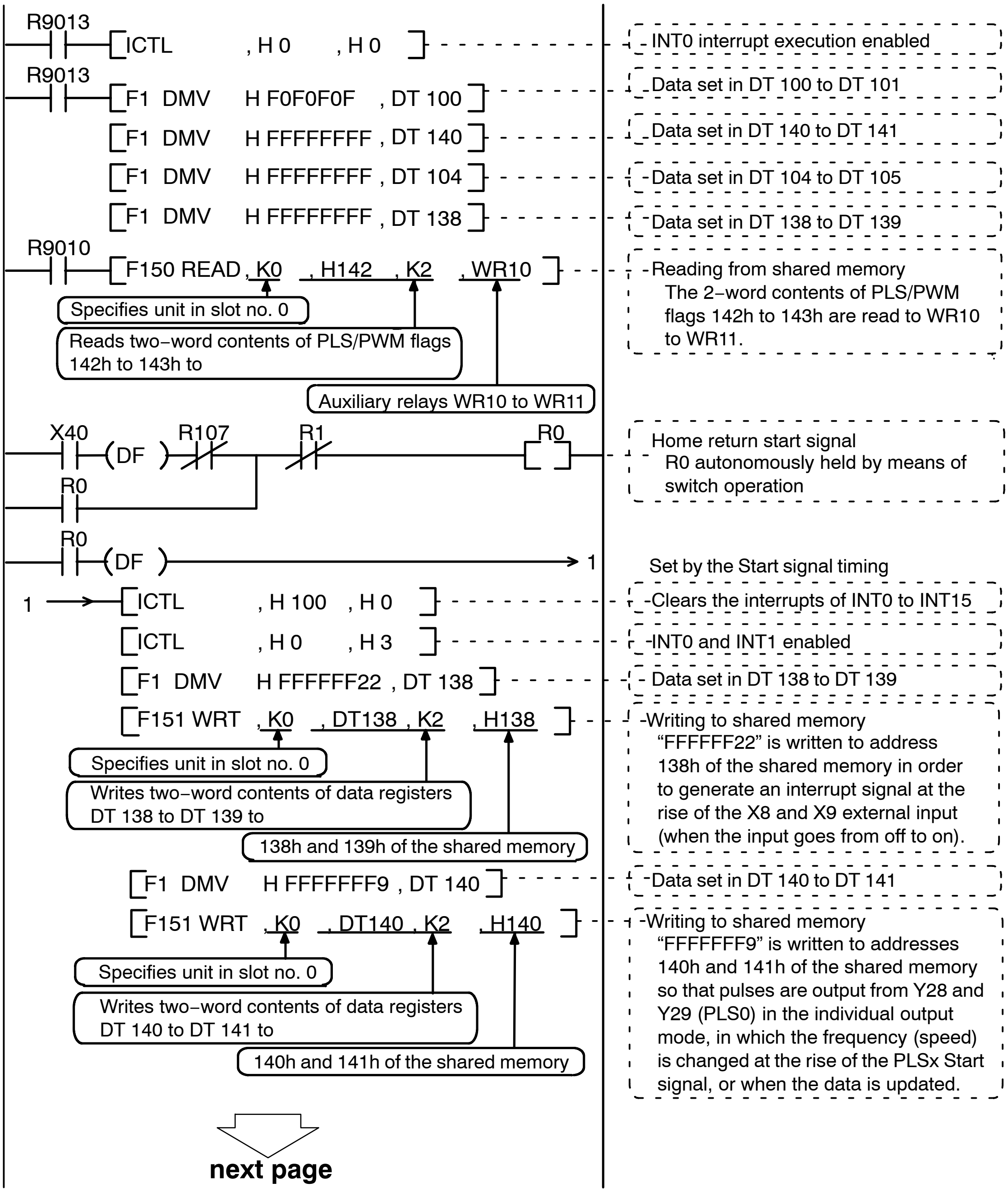
The PLS/PWM frequency setting is used to specify the frequency of the pulses.
In the exmaple shown here, pulses are being output from Y28 and Y29 (PLS0) at 2kHz, so a value of “K 2000(H 7D0)” should be written to addresses 148h and 149h of the shared memory. This data is rewritten to “K1000(H 3E8)” at the timing at which the home near input (X8) goes on.

Setting of shared memory addresses 148h and 149h

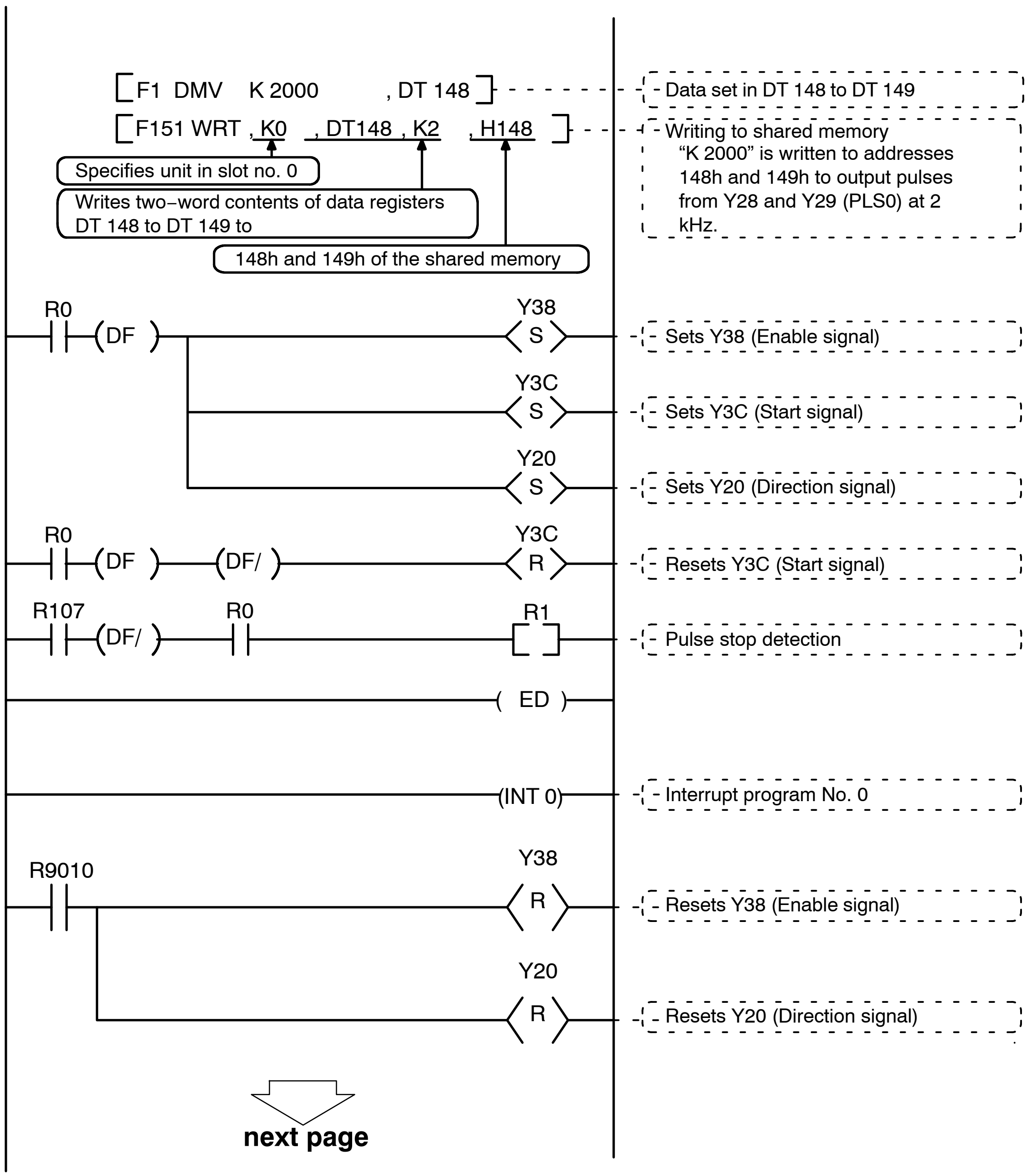
(bit)	32			16	15			0
Setting item	PLS0/PWM0 frequency setting							
Set value	0	0	0	0	0	7	D	0
Setting contents (Decimal)	K2000							

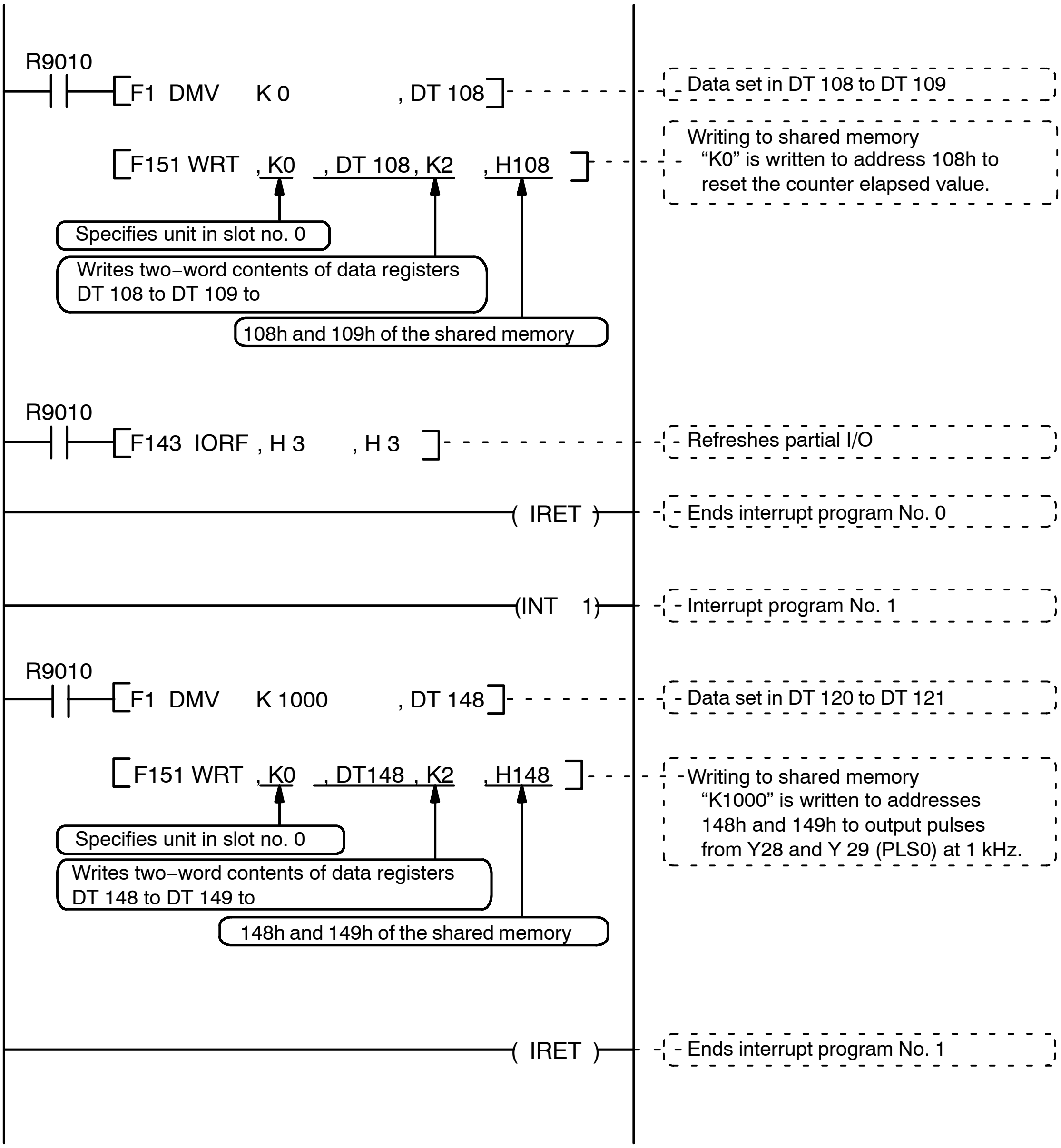
10.6.5 Sample Program

“FFFFFF22” is written to the interrupt setting area (138h and 139h) of the shared memory addresses to set an interrupt at the rise of the external input of X8 and X9 (when the external input goes from off to on). The program is structured so that interrupts are enabled prior to the End instruction, and are executed after the End instruction.
Also, settings concerning the pulse output function and programs concerning pushbutton operation are described.



10.6 Home Return Using the Pulse Output Function




R9010
F1 DMV K 0 , DT 108
Data set in DT 108 to DT 109
F151 WRT , K0 , DT 108 , K2 , H108
Writing to shared memory
“K0” is written to address 108h to reset the counter elapsed value.
Specifies unit in slot no. 0
Writes two–word contents of data registers DT 108 to DT 109 to
108h and 109h of the shared memory
R9010
F143 IORF , H 3 , H 3
Refreshes partial I/O
IRET
Ends interrupt program No. 0
INT 1
Interrupt program No. 1
R9010
F1 DMV K 1000 , DT 148
Data set in DT 120 to DT 121
F151 WRT , K0 , DT148 , K2 , H148
Writing to shared memory
“K1000” is written to addresses 148h and 149h to output pulses from Y28 and Y 29 (PLS0) at 1 kHz.
Specifies unit in slot no. 0
Writes two–word contents of data registers DT 148 to DT 149 to
148h and 149h of the shared memory
IRET
Ends interrupt program No. 1

Chapter 11

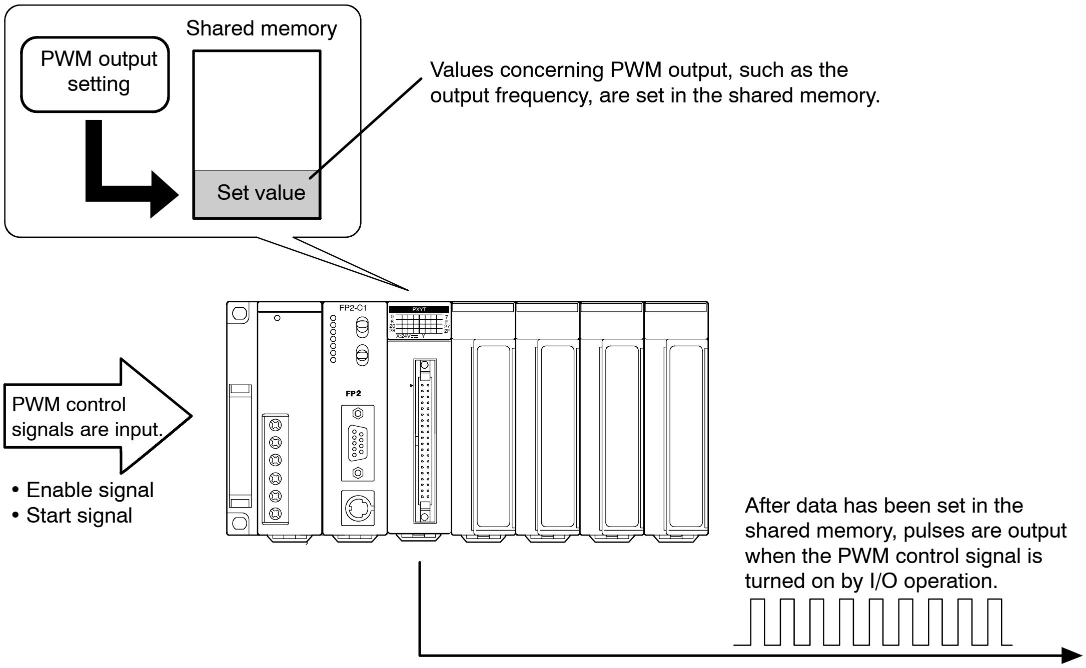
Using the PWM Output Function (Only for Pulse I/O Unit)

11.1 About the PWM Output Function

11.1.1 What is the PWM Output Function?

The PWM output function outputs a duty of any desired frequency within a range of 0% and 100%. Settings can be entered in units of 1%.
Any desired frequency between 1 Hz and 30 kHz can be entered in units of 1 Hz.

Also, the FP2 Pulse I/O Unit can output PWM on up to four channels. Because the pulse output function and the PWM output function can both be selected, however, there will be fewer channels available for use with the PWM output function if the pulse output function is also being used.



Note

The four channels listed below are used for pulse−related output (pulse output and PWM output):

– Channel 0: PLS0 output or PWM0 output

– Channel 1: PLS1 output or PWM1 output

– Channel 2: PLS2 output or PWM2 output

– Channel 3: PLS3 output or PWM3 output

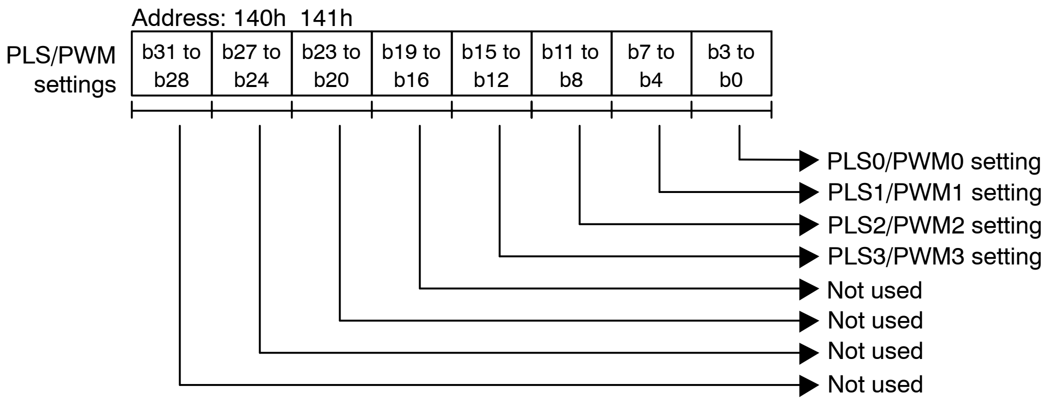
11.1.2 Entering Settings for the PWM Output Function

Using the pulse output function involves entering PLS/PWM settings in the shared memory (Procedure 1), setting the PLS/PWM frequency settings in the shared memory (Procedure 2), and setting the PWM duty in the shared memory (Procedure 3).

In addition to the shared memory settings, control of the Enable, Start and Direction signals is necessary using the PLS control signal.

Procedure 1: PLS/PWM settings in the shared memory

The PWM output type is specified using the PLS/PWM setting in the shared memory.



Pulse output settings (PWM, PLS)

Set value (HEX)	Function		
	Pulse function	**Timing at which data changes**	**Output mode**
0	PWM	Updated at rise of PLSx start signal	—
1		At rise of PLSx start signal, or on comparison output	
2		At rise of PLSx start signal, or when data is updated	
3		Reserved as spare	
4	PLS	Updated at rise of PLSx start signal	Direction control
5			Individual output
6		At rise of PLSx start signal, or on comparison output	Direction control
7			Individual output
8		At rise of PLSx start signal, or when data is updated	Direction control
9			Individual output
A	Invalid *1	Invalid *1	Invalid *1
B			
C			
D			
E			
F	Not used *2	—	—

*1: No settings should be entered.
*2: When the power supply is turned on, the default value of “Not used” is set for this.

Note

The shared memory should always be accessed in two−word units.

◆ REFERENCE

For information on shared memory addresses, see page 13 – 12.

Procedure 2: PLS/PWM frequency settings in the shared memory

After the PLS/PWM settings have been set in the shared memory, the frequency of the output pulses should be specified.

A value between 1 Hz and 30 kHz should be specified, in units of 1 Hz.
If a value of 31.458 kHz or higher is specified, the output goes off (pulses are stopped).

If 0 Hz is set for the set value and the data is updated, pulse output stops.

	Address	
PLS0/PWM0 frequency setting	148h 149h	For PWM: K0 to K30000
PLS1/PWM1 frequency setting	14Ah 14Bh	For PWM: K0 to K30000
PLS2/PWM2 frequency setting	14Ch 14Dh	For PWM: K0 to K30000
PLS3/PWM3 frequency setting	14Eh 14Fh	For PWM: K0 to K30000

Procedure 3: PWM duty setting in the shared memory

After the PLS/PWM frequency setting has been entered in the shared memory, specify the duty of the output pulses.

The set value can be any value between 0% and 100%, and can be set in units of 1%.
The set value indicates the on percentage.

When a value of 0% is set, the output will be turned off, and when 100% is set, the output will be turned on. When a value of 101% or higher is set, the output will be turned off.

	Address	
PWM0 Duty setting	158h 159h	K0 to K100
PWM1 Duty setting	15Ah 15Bh	K0 to K100
PWM2 Duty setting	15Ch 15Dh	K0 to K100
PWM3 Duty setting	15Eh 15Fh	K0 to K100

Notes

- **The shared memory should always be accessed in two−word units.**
- **If 0 Hz (K0) is set, no pulses are output.**
- **To avoid malfunctions, make sure the values set do not exceed the rated values.**
- **The upper limit for error detection in the PWM frequency setting is 41.943 kHz. The upper limit for error detection in the duty setting is 127%. Setting a value which exceeds either of these prevents normal operation.**
  For more detailed information, see page 1 – 16.

Procedure 4: PWM control signals

After the shared memory settings have been entered, control of the Enable and Start signals is necessary using the PWM control signal.

Enable signal

The Enable signal controls whether PWM output is valid or to be stopped.

on: PWM output is valid.
off: PWM output stops.

Start signal

The Start signal initiates PWM output and changes the pulse frequency and duty.
The frequency and duty can also be changed by manipulating the timing of the “Comparison Matching” and “Data Update” parameters, under the “Pulse output settings”.

This signal is valid only when the Enable signal is on, and becomes invalid if the Enable signal goes off. Pulse output is enabled when both the Enable signal and the Start signal go on at the same time.

When Start signal goes on for first time: PWM output begins.
At leading edge (off → on): Output pulse frequency and duty are changed.

The table below shows the output allocations for the various control signals.

Table of control signal allocations

<table>
<tr><th rowspan="2">Output allocation</th><th colspan="3">Function</th></tr>
<tr><th>Pulse output CH</th><th colspan="2">Control content</th></tr>
<tr><td>Y38</td><td>PWM0</td><td rowspan="4">Enable control</td><td rowspan="4">When off: PWM output stops
When on: PWM output is valid</td></tr>
<tr><td>Y39</td><td>PWM1</td></tr>
<tr><td>Y3A</td><td>PWM2</td></tr>
<tr><td>Y3B</td><td>PWM3</td></tr>
<tr><td>Y3C</td><td>PWM0</td><td rowspan="4">Start control</td><td rowspan="4">When first on: PWM output begins
At leading edge (off → on): Output pulse frequency and duty are changed</td></tr>
<tr><td>Y3D</td><td>PWM1</td></tr>
<tr><td>Y3E</td><td>PWM2</td></tr>
<tr><td>Y3F</td><td>PWM3</td></tr>
</table>

Notes

- **The pulse control signals and PWM control signals are allocated to the same function in the same location.**
- **The PLS/PWM setting should be entered in the shared memory first, followed by the PLS/PWM frequency setting and then the PWM duty setting. Reversing the sequence can interfere with normal operation.**
- **If the frequency and/or duty was changed during PWM output, the setting is updated at the timing when the next waveform is output, after the current waveform has been output.**
- **Please be aware that, if the Enable signal is turned off during PWM output, the PWM output goes off at that point.**

◆ **REFERENCE**

PLS/PWM flags are available at addresses 142h and 143h of the shared memory. Reading the statuses of the flags at these addresses enables monitoring of pulse output. For more information, see page 13 – 26.

11.1.3 Timing at Which Changes are Reflected in Output When Data is Changed

Timing at which data is changed

With the Pulse I/O Unit, the three modes described below are provided as the timing at which output frequency data is updated.

1. Data is updated at the rise of the PLS Start signal.
   In this mode, the frequency value (duty value) to be changed is written to the shared memory ahead of time, and the data is updated at the point when the PLS Start signal goes from off to on.

2. Data is updated when the results of a comparison are output.
   In this mode, the frequency value (duty value) to be changed is written to the shared memory ahead of time, and the data is updated at the point when the counter elapsed value matches the comparison value.

3. Data is updated when the data is refreshed.
   In this mode, the data is updated when the frequency value (duty value) to be changed is written to the shared memory.

Timing at which changes are reflected in output

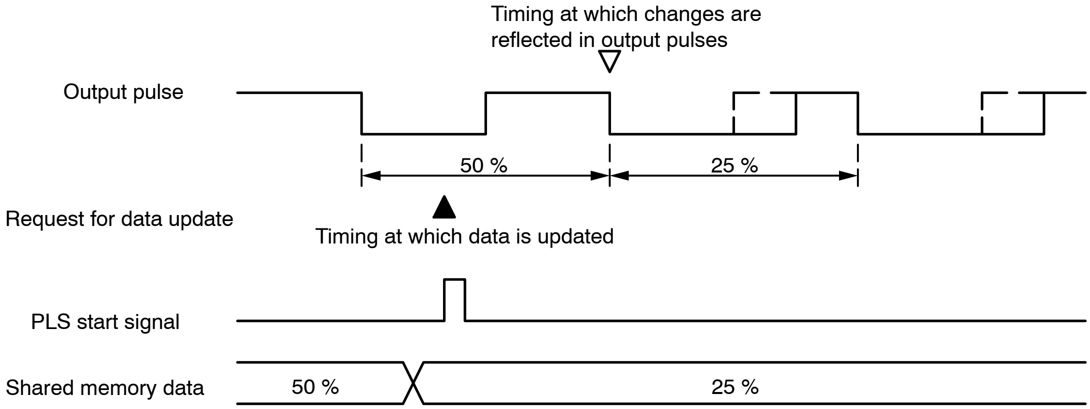
Frequency values (duty values) updated at the timing described above are reflected at the next fall of the pulse being output.
For more detailed information, please see the timing chart on the following page.

☞ **Note**

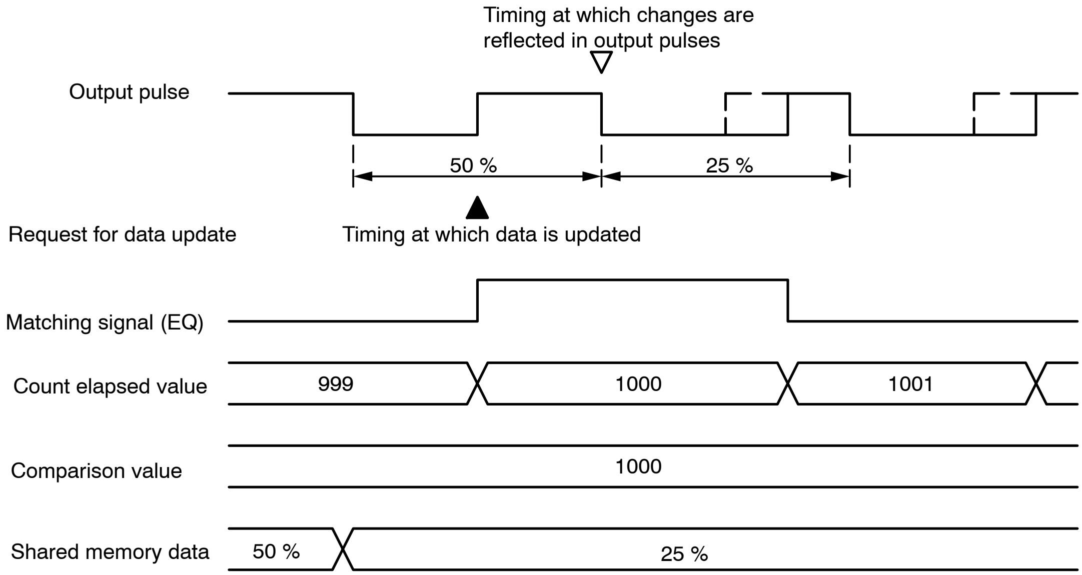
Data updated when the data was changed is reflected at the next fall of the pulse being output. Please be aware that this means, if data was updated several times during one cycle, the most recent data changes will be reflected.

Timing chart

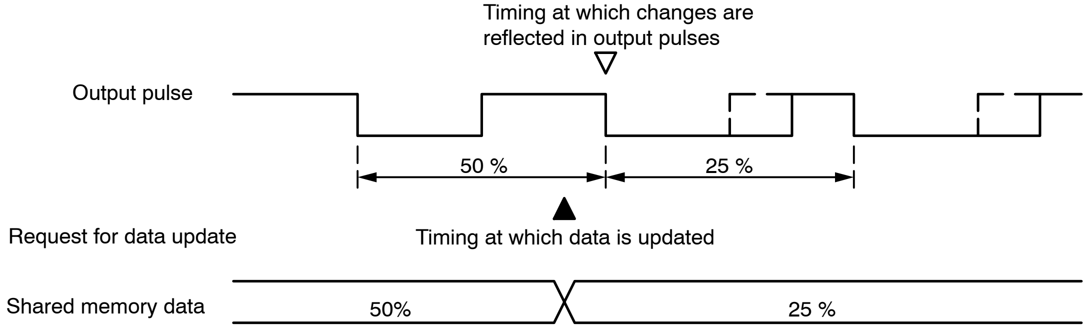
Data refreshed at rise of PLS Start signal



Data updated on comparison output



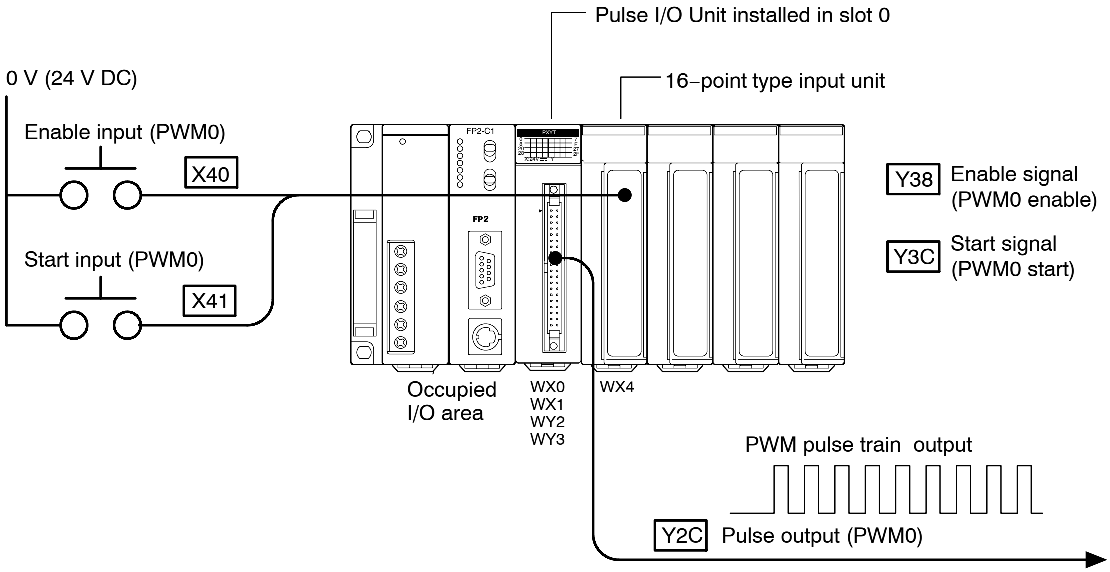
Data updated when data is changed



* Changes in the frequency also take place at the same timing as that described above.

11.2 Using the PWM Output Function

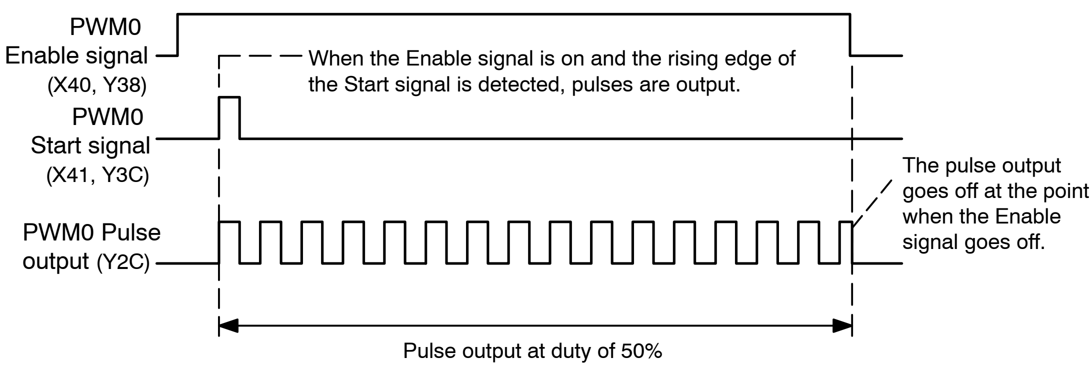
11.2.1 Overview



PWM is output. When the Enable input (X40) is turned on and the Start input goes on, PWM is output from Y2C (PWM0).

11.2.2 Timing Chart

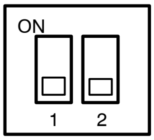
The following shows changes in the PWM output in response to the input statuses of the various signals.



11.2.3 Setting the Mode Setting Switches

Mode A should be set if no interrupts are being used.

Mode A (SW1 → off, SW2 → off)



No interruption

When this setting is used, the interrupt function will not operate even if used.

The PWM output function can be used regardless of whether the interrupt function is set to “Used” or “Not Used”.

11.2.4 Shared Memory Settings

PLS/PWM setting

The PLS/PWM setting is used to specify the PWM output type.
In the example shown here, the PWM is being output from Y2C (PWM0) in the mode in which data is updated at the rise of the PLSx Start signal, so a value of “FFFFFFF0” should be written to addresses 140h and 141h of the shared memory.

Setting of shared memory addresses 140h and 141h

(bit)	32			16	15			0
Output number	Not used	Not used	Not used	Not used	PWM3	PWM2	PWM1	PWM0
Setting item	Not used	Not used	Not used	Not used	Type setting	Type setting	Type setting	Type setting
Set value	F	F	F	F	F	F	F	0
Setting contents (Function)	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Data updated at Start signal

PLS/PWM frequency setting

The PLS/PWM frequency setting is used to specify the frequency of the PWM output.
In the example shown here, the PWM is being output from Y2C (PWM0) at 10 kHz, so a value of “K 10000 (H 2710)” should be written to addresses 148h and 149h of the shared memory.

Setting of shared memory addresses 148h and 149h

(bit)	32			16	15			0
Setting item	PLS0/PWM0 frequency setting							
Set value (HEX)	0	0	0	0	2	7	1	0
Setting contents (Decimal)	K10000							

PWM duty setting

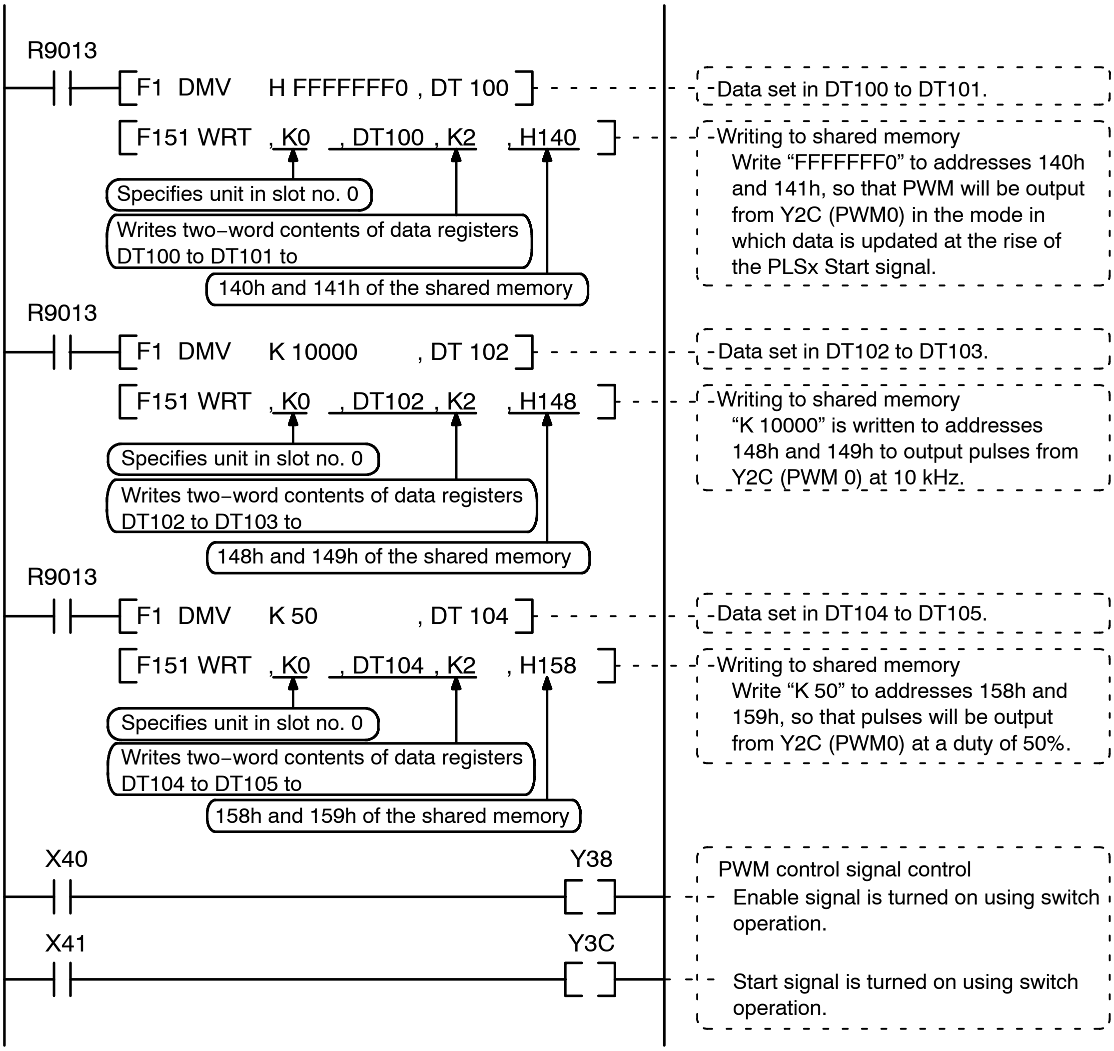
The duty of the PWM output is specified using the PWM duty setting.
In the example shown here, the PWM is being output from Y2C (PWM0) at a duty ratio of 50%, so a value of “K 50 (H 32)” should be written to addresses 158h and 159h of the shared memory.

Setting of shared memory addresses 158h and 159h

(bit)	32			16	15			0
Setting item	PWM0 duty setting							
Set value (HEX)	0	0	0	0	0	0	3	2
Setting contents (Decimal)	K50							

11.2.5 Sample Program

The settings relating to the PWM output are entered in the shared memory, and then pushbutton operation is used to output the PWM.



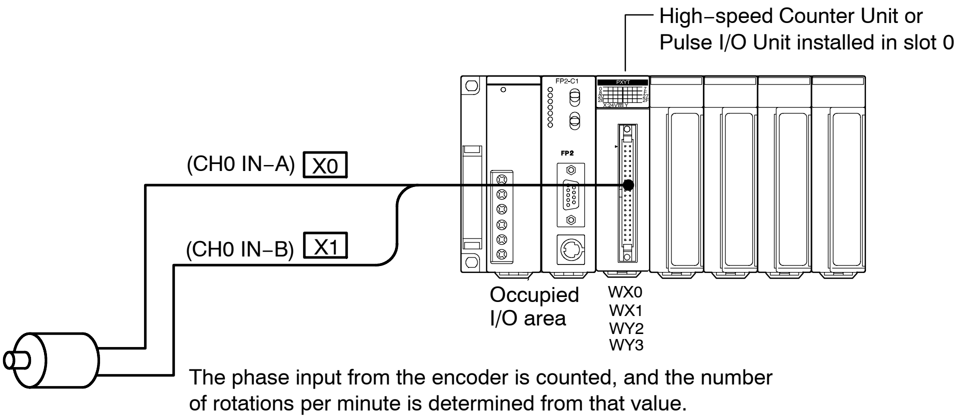
Chapter 12

Sample Programs

☛ next page

12.1 Speed Calculation

12.1.1 Overview



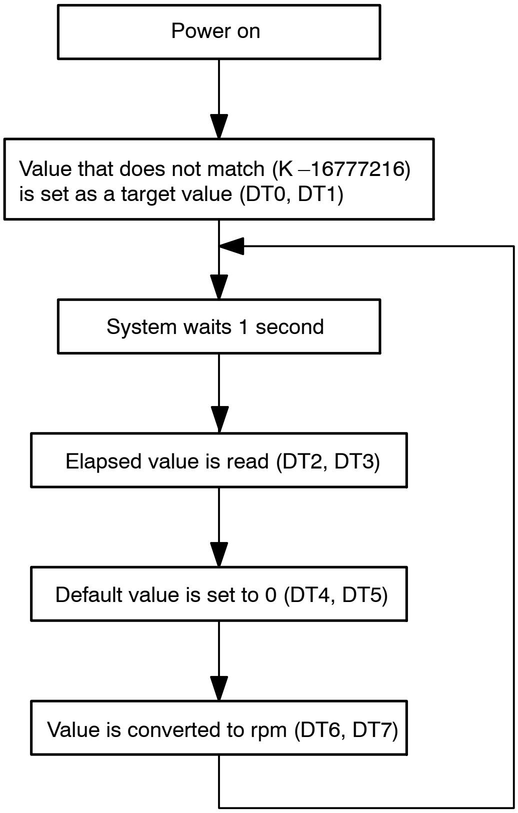
Calculation formula for determining the number of rotations per minute

$$\text{No. of rotations per minute} = \frac{\text{No. of pulses per second}}{\text{No. of pulses per rotation}} \times 60 = \frac{\text{No. of pulses per second} \times 60}{1000}$$

$$= \text{No. of pulses per second} \times \frac{3}{50}$$

The phase signals from the encoder are input to X0 and X1, and the number of counts per second is calculated. In the example shown here, the encoder resolution is 1,000 pulses per rotation.
After the calculation has been made, the value indicating the speed per minute is stored in DT6 and DT7, and can be confirmed using the “Monitor Function” programming tool in the FPWIN GR or a similar program.

12.1.2 Flowchart



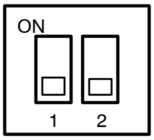
Tip

The phase differential input mode has a multiplier function that can be used to change the multiplication ratio of the input pulses.
For detailed information, see page 1 – 9.

12.1.3 Setting the Mode Setting Switches

Specify “Mode A” to use only the counter function, without using interrupts.

Mode A (SW1 → off, SW2 → off)



No interruption

When this setting is used, the interrupt function will not operate even if used.

The counter function can be used regardless of whether the interrupt function is set to “Used” or “Not Used”.

12.1.4 Shared Memory Settings

Counter Setting

This sets the operation modes for each counter channels.
In this example, phase signals such as encoders are input to X0 and X1, and the counter function is used with the multiplication phase input mode.
Therefore, a value of “FFFFFF20” should be written to addresses 100h and 101h of the shared memory.

Setting of shared memory addresses 100h and 101h

(bit)	32			16	15			0
External input	XD	XC	X9	X8	X5	X4	X1	X0
Counter number	CH3		CH2		CH1		CH0	
Setting item	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting
Set value	F	F	F	F	F	F	2	0
Setting contents (Function)	Not used	Not used	Not used	Not used	Not used	Not used	Phase input	Terminal input

Setting the counter elapsed value

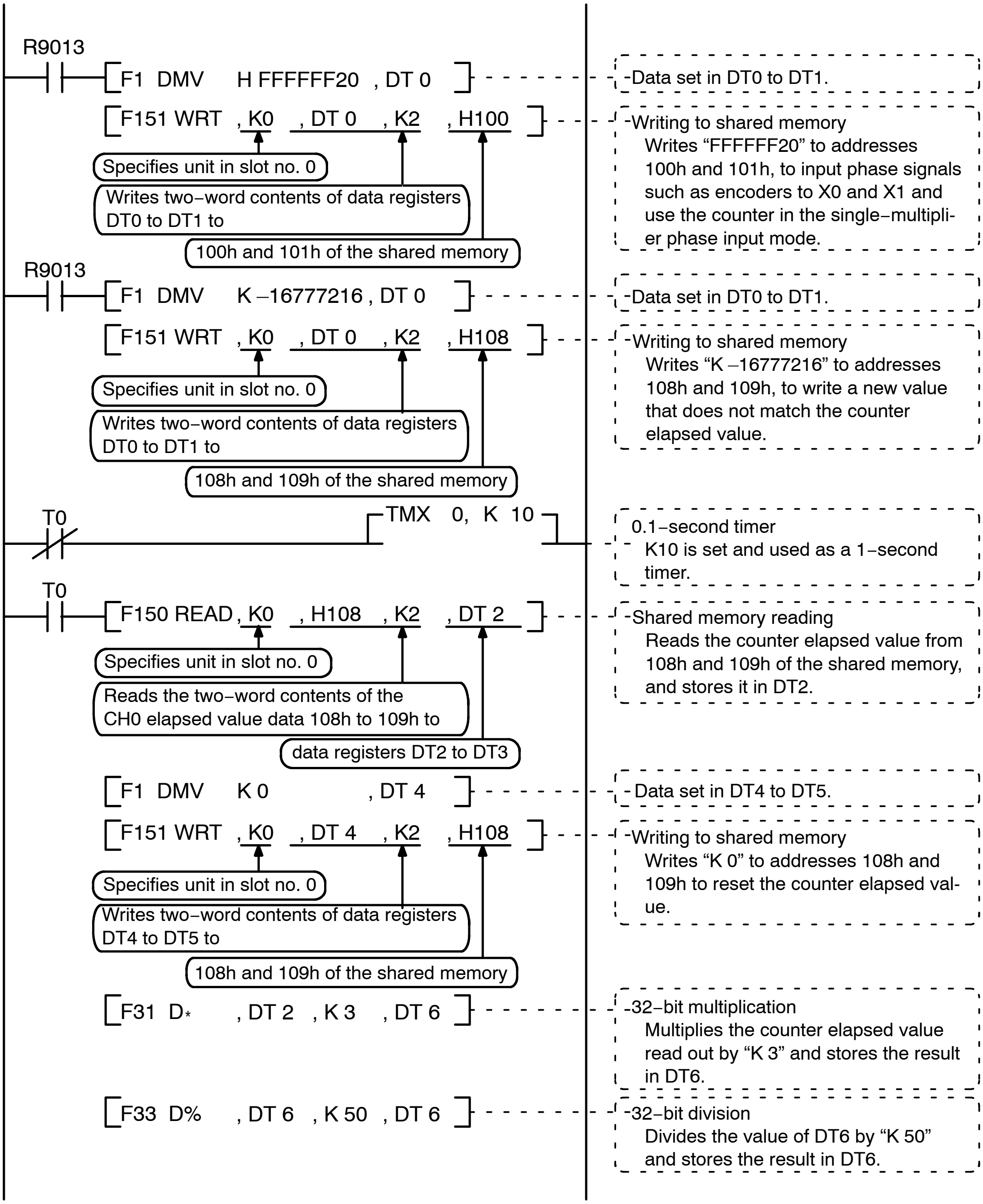
Write a value that does not match the counter elapsed value of CH0.
In the example shown here, a value of “K –16777216 (H FF000000)” should be written to addresses 108h and 109h of the shared memory in which the elapsed value is stored.

Setting contents of shared memory addresses 108h and 109h

(bit)	32			16	15			0
Setting item	Comparison output set value (for CMP0)							
Set value (HEX)	F	F	0	0	0	0	0	0
Setting contents (Decimal)	K –16777216							

12.1.5 Sample Programs

This program writes a value of “FFFFFF20” to the counter setting area (100h, 101h) of the shared memory addresses, inputs phase signals from an encoder or similar unit to X0 and X1, and determines the number of rotations per minute from that value.

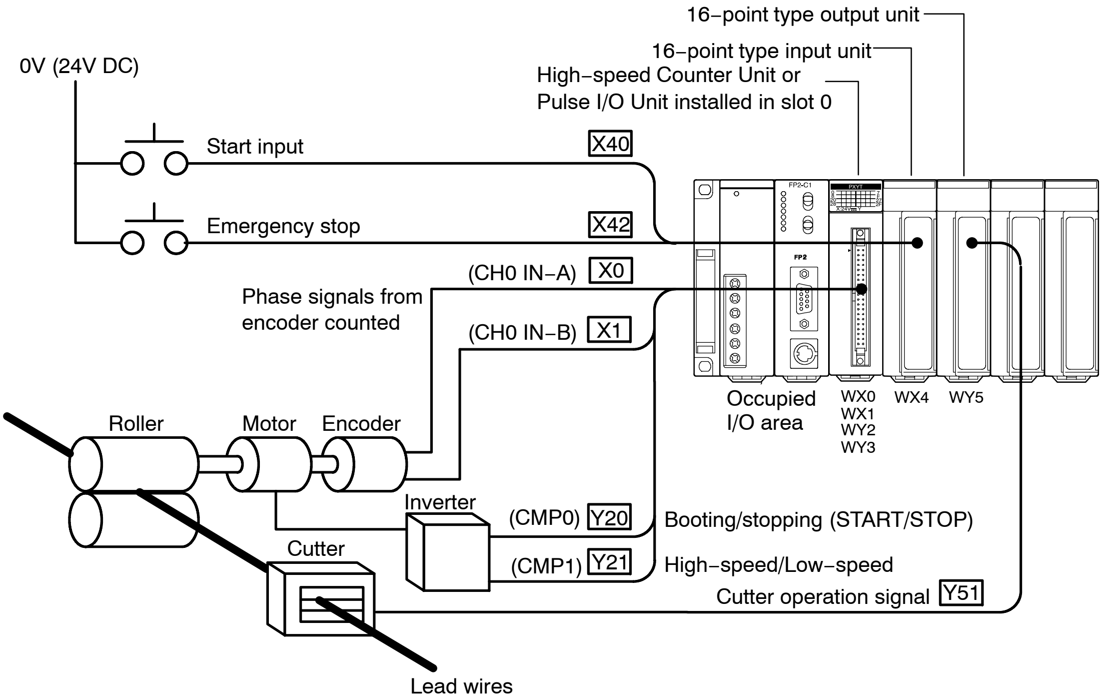


Values stored in data registers

Address	Content
DT0, DT1	Target value
DT2, DT3	Current value (elapsed value)
DT4, DT5	Default value (0)
DT6, DT7	Speed (rpm)

12.2 Processing of Specific Lengths of Wire

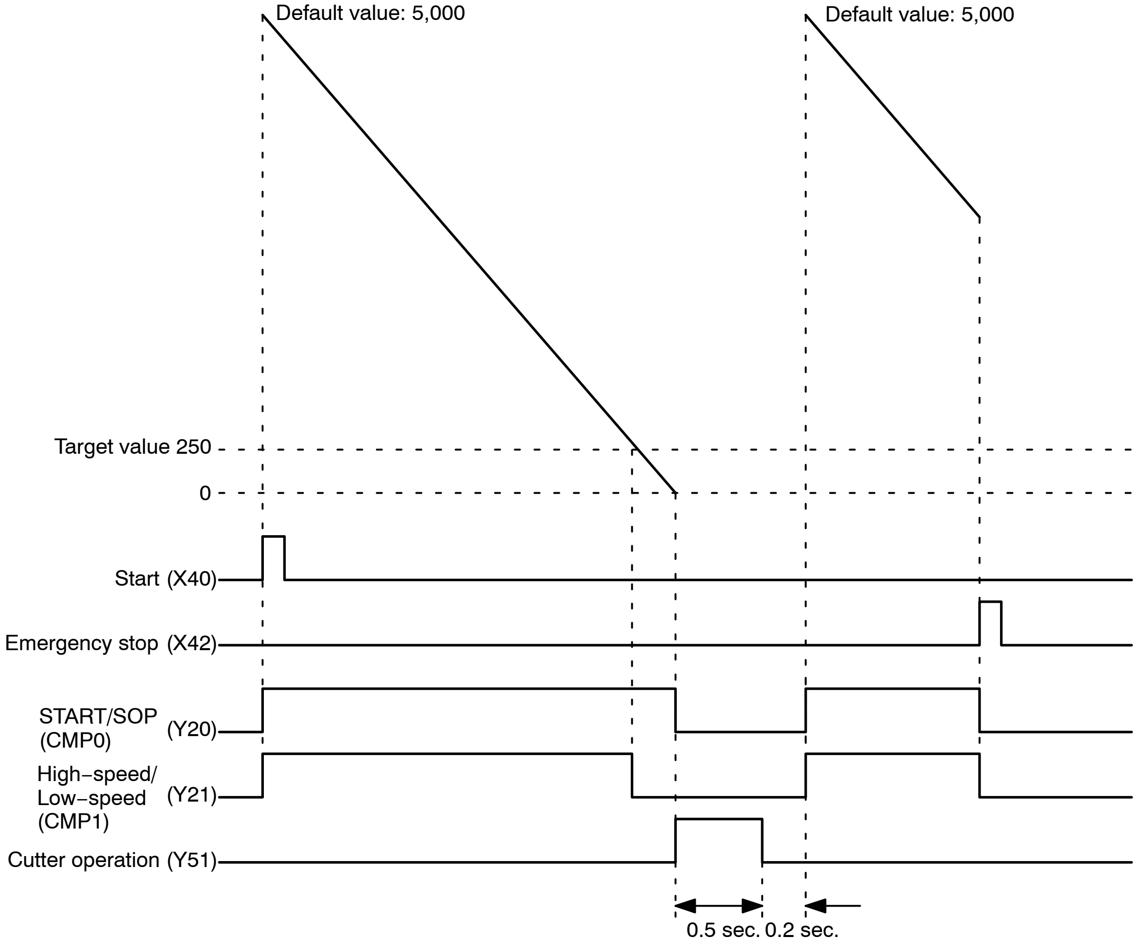
12.2.1 Overview



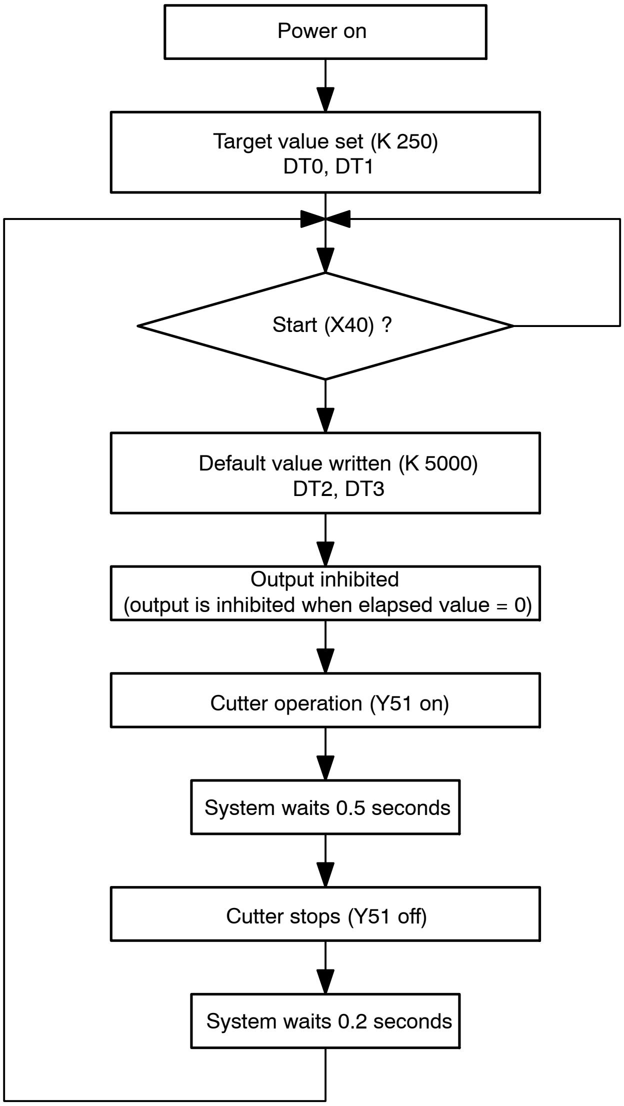
In the example shown here, a feed roller with an outer periphery of 10 cm is used, that makes the lead wire advance 10 cm for each rotation.
Using this roller, the feed speed is decreased at the point where 95 cm of lead wire has been fed, and the roller stops when 100 cm has been fed (ten rotations). In this example, the encoder resolution is 500 pulses per rotation.
Also, rather than pulse output being used, the inverter is started and stopped using the CMP0 signal, and the CMP1 signal is used for high/low speed control.

12.2.2 Timing Chart

The following shows changes in the count value and output that occur in response to the input statuses of the various signals.



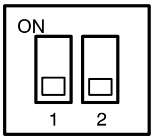
12.2.3 Flowchart



12.2.4 Setting the Mode Setting Switches

Specify “Mode A” to use only the counter function, without using interrupts.

Mode A (SW1 → off, SW2 → off)



No interruption

When this setting is used, the interrupt function will not operate even if used.

The counter function can be used regardless of whether the interrupt function is set to “Used” or “Not Used”.

Tip

The phase differential input mode has a multiplier function that can be used to change the multiplication ratio of the input pulses.
For detailed information, see page 1 – 9.

12.2.5 Shared Memory Settings

Counter Setting

This sets the operation modes for the various counter channels.
In this example, phase signals such as encoders are input to X0 and X1, and the counter function is used with the multiplication phase input mode.
Therefore, a value of “FFFFFF20” should be written to addresses 100h and 101h of the shared memory.

Setting of shared memory addresses 100h and 101h

(bit)	32			16	15			0
External input	XD	XC	X9	X8	X5	X4	X1	X0
Counter number	CH3		CH2		CH1		CH0	
Setting item	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting
Set value	F	F	F	F	F	F	2	0
Setting contents (Function)	Not used	Not used	Not used	Not used	Not used	Not used	Phase input	Terminal input

Setting the Counter Elapsed Value

Write “K 5000 (H 1388)” as the default value to addresses 108h and 109h of the shared memory in which the counter elapsed value for CH0 is stored.

Setting of shared memory addresses 108h and 109h

(bit)	32			16	15			0
Setting item	Comparison output set value (for CMP0)							
Set value (HEX)	0	0	0	0	1	3	8	8
Setting contents (Decimal)	K 5000							

Setting the Comparison Output Set Value

Here, the comparison output set value, which is compared to the counter elapsed value, is set.
The example shown here is set up so that CMP0 is output when the counter elapsed value reaches 0, and CMP1 is output when the value reaches 250, so write “K 0 (H 0)” to addresses 120h and 121h, and “K 250 (H FA)” to addresses 122h and 123h of the shared memory.

Setting of shared memory addresses 120h and 121h

(bit)	32			16	15			0
Setting item	Comparison output set value (for CMP0)							
Set value (HEX)	0	0	0	0	0	0	0	0
Setting contents (Decimal)	K 0							

Setting of shared memory addresses 122h and 123h

(bit)	32			16	15			0
Setting item	Comparison output set value (for CMP1)							
Set value (HEX)	0	0	0	0	0	0	F	A
Setting contents (Decimal)	K 250							

Comparison Output Setting

The channel number and output logic for the counter used in the comparison output function are selected.
In the example shown here, the counter elapsed value for CH0 is compared with the comparison output set value and the comparison results are output to CMP0 and CMP1. Write “FFFFFF44” or “FFFFFF00” to addresses 104h and 105h of the shared memory.

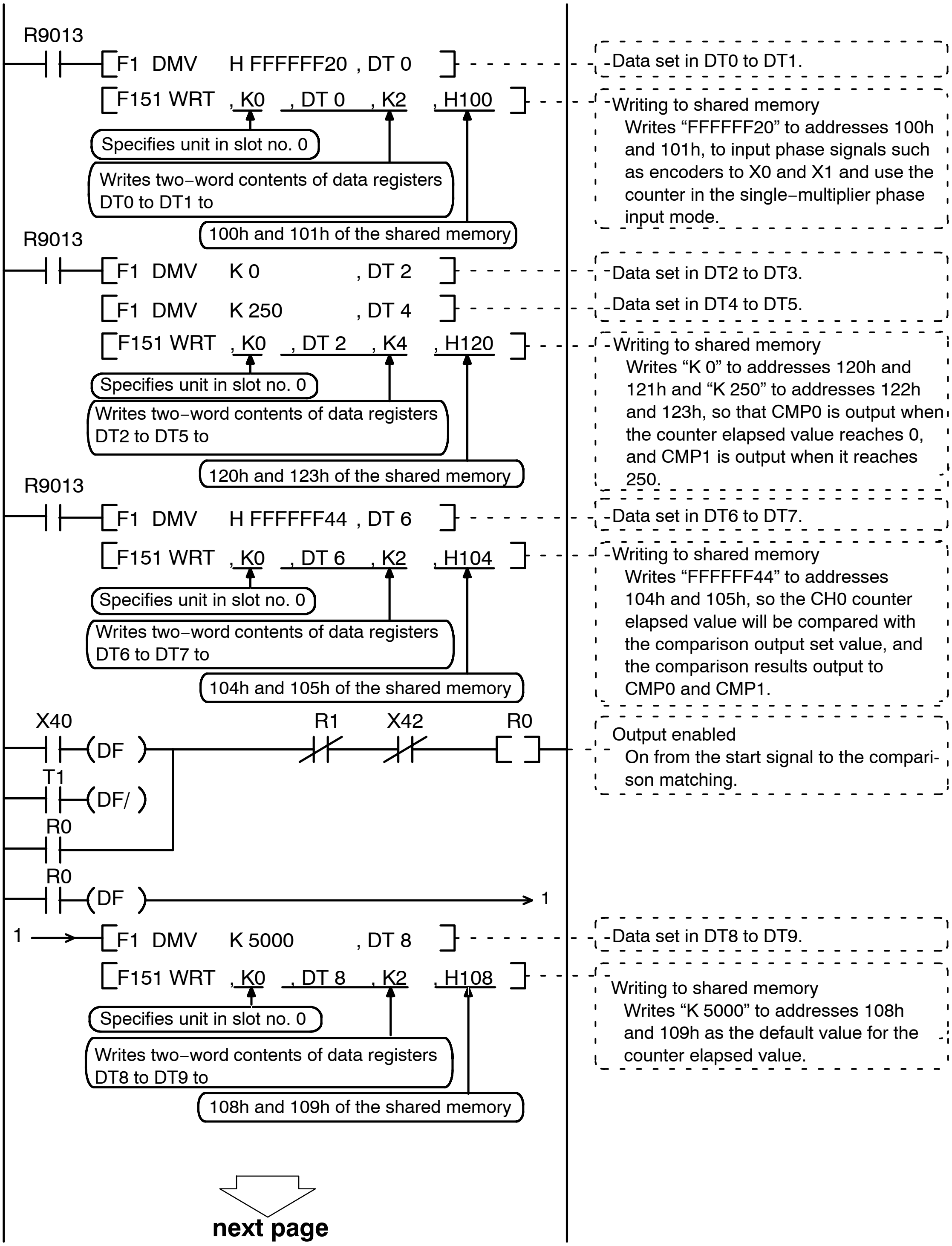
Setting of shared memory addresses 104h and 105h

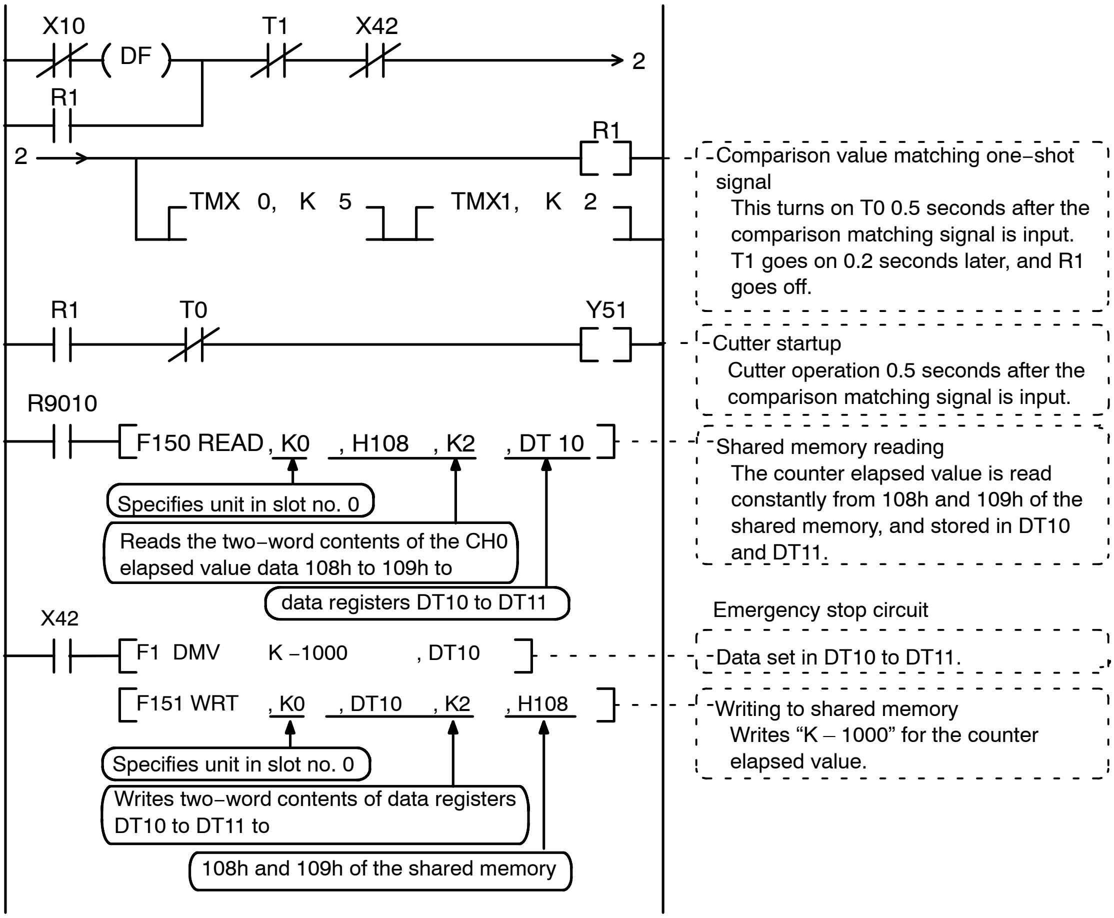
(bit)	32			16	15			0
Comparison output	CMP7	CMP6	CMP5	CMP4	CMP3	CMP2	CMP1	CMP0
Set value	F	F	F	F	F	F	4	4
Setting contents (Function)	Not used	Not used	Not used	Not used	Not used	Not used	CH0 comparison*	CH0 comparison*

* Goes on if the elapsed value is more than or equal to the set value

12.2.6 Sample Programs

This program enters settings relating to the counter and comparison functions, and settings relating to pushbutton operation, in the shared memory.



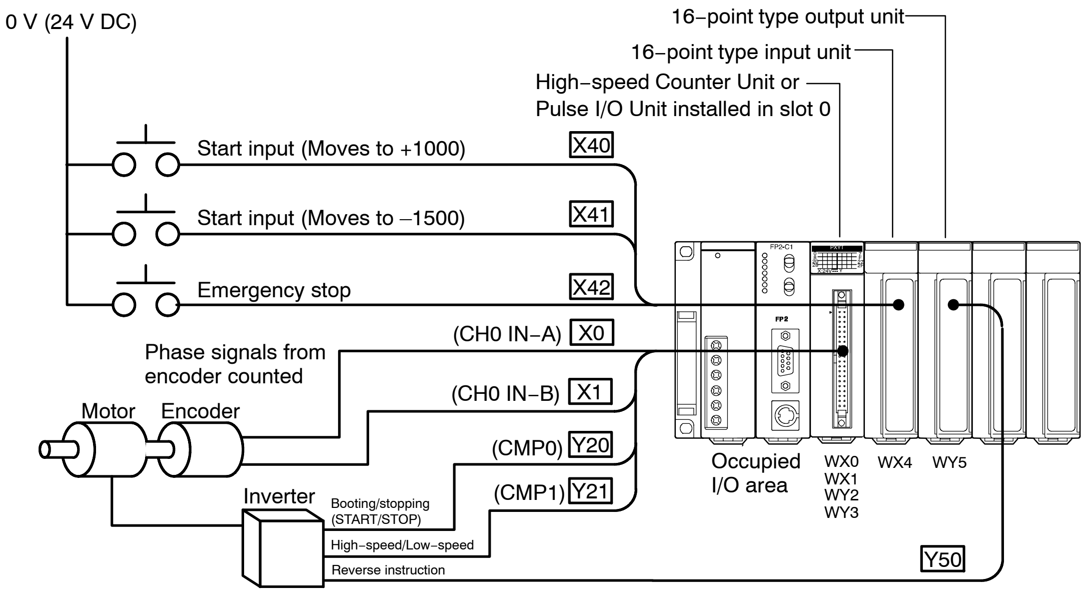


Values stored in data registers

Address	Content
DT2 to DT4	Target value
DT8, DT9	Default value
DT10, DT11	Current value (elapsed value)

12.3 Position Control Using Absolute Values

12.3.1 Overveiw

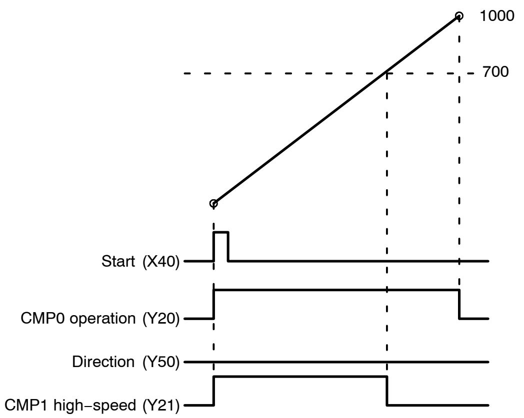


Absolute values are used for positioning control. A shift is made to +1000 when X40 is input, and to –1500 when X41 is input. The speed decreases 300 pulses before the stopping position, and the system stops.
Also, rather than pulse output being used, the inverter is started and stopped using the CMP0 signal, and the CMP1 signal is used for high/low speed control.

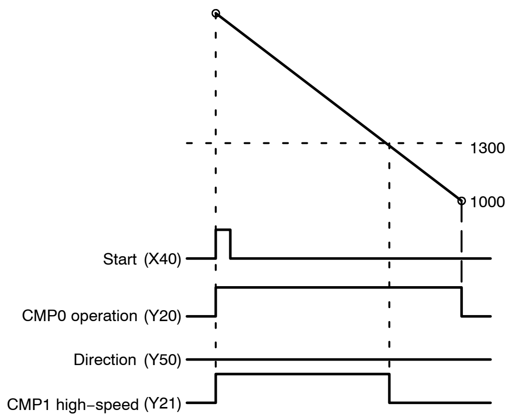
12.3.2 Timing Chart

The following shows changes in the count value and output that occur in response to the input statuses of the various signals.

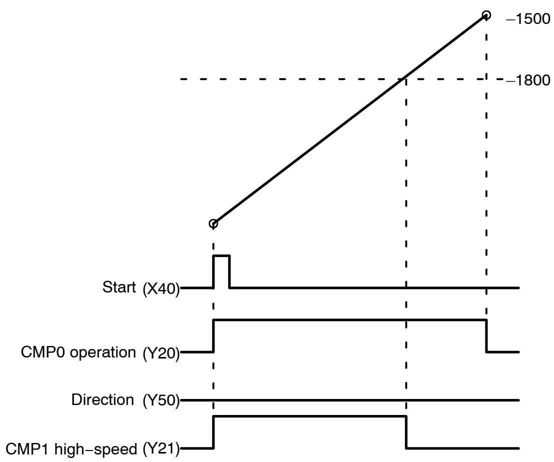
X40 goes on and target value is K1000
(current value < target value)



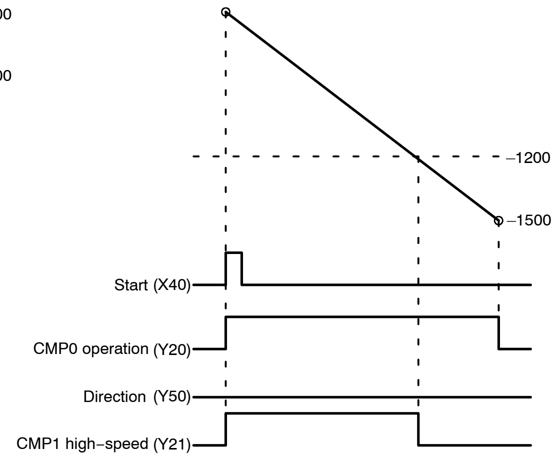
X40 goes on and target value is K1000
(current value > target value)



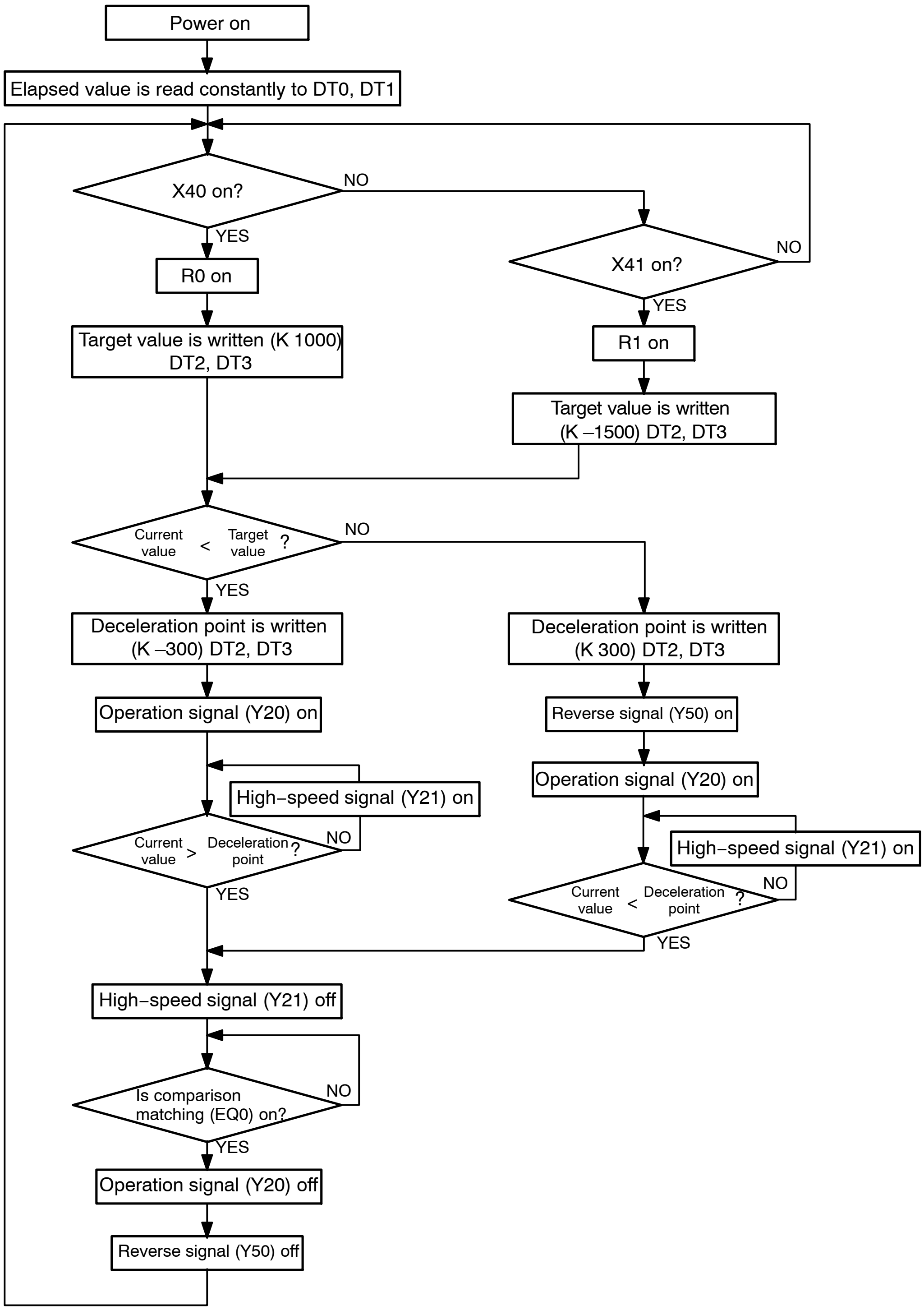
X41 goes on and target value is K–1500
(current value < target value)



X41 goes on and target value is K–1500
(current value > target value)



12.3.3 Flowchart



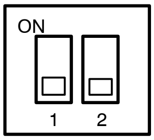
Tip

The phase differential input mode has a multiplier function that can be used to change the multiplication ratio of the input pulses.
For detailed information, see page 1 – 9.

12.3.4 Setting the Mode Setting Switches

Specify “Mode A” to use only the counter function, without using interrupts.

Mode A (SW1 → off, SW2 → off)



No interruption

When this setting is used, the interrupt function will not operate even if used.

The counter function can be used regardless of whether the interrupt function is set to “Used” or “Not Used”.

12.3.5 Shared Memory Settings

Counter Setting

This sets the operation modes for each counter channels.
In this example, phase signals such as encoders are input to X0 and X1, and the counter function is used with the multiplication phase input mode.
Therefore, a value of “FFFFFF20” should be written to addresses 100h and 101h of the shared memory.

Setting of shared memory addresses 100h and 101h

(bit)	32			16	15			0
External input	XD	XC	X9	X8	X5	X4	X1	X0
Counter number	CH3		CH2		CH1		CH0	
Setting item	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting
Set value	F	F	F	F	F	F	2	0
Setting contents (Function)	Not used	Not used	Not used	Not used	Not used	Not used	Phase input	Terminal input

Setting the Comparison Output Set Value

Here, the comparison output set value, which is compared to the counter elapsed value, is set.
In the example shown here, "K 1000 (H 3E8)" is written to addresses 120h and 121h of the shared memory when X40 goes on, and "K –1500 (H FFFFFA24)" to addresses 120h and 121h when X41 goes on.

Setting of shared memory addresses 120h and 121h

X40 goes on

(bit)	32			16	15			0
Setting item	Comparison output set value (for CMP0)							
Set value (HEX)	0	0	0	0	0	3	E	8
Setting contents (Decimal)	K 1000							

X41 goes on

(bit)	32			16	15			0
Setting item	Comparison output set value (for CMP0)							
Set value (HEX)	F	F	F	F	F	A	2	4
Setting contents (Decimal)	K –1500							

Comparison Output Setting

The channel number and output logic for the counter used in the comparison output function are selected.
In the example shown here, the counter elapsed value for CH0 is compared with the comparison output set value and the comparison results are output to CMP0 and CMP1. Write "FFFFFF44" or "FFFFFF00" to addresses 104h and 105h of the shared memory.

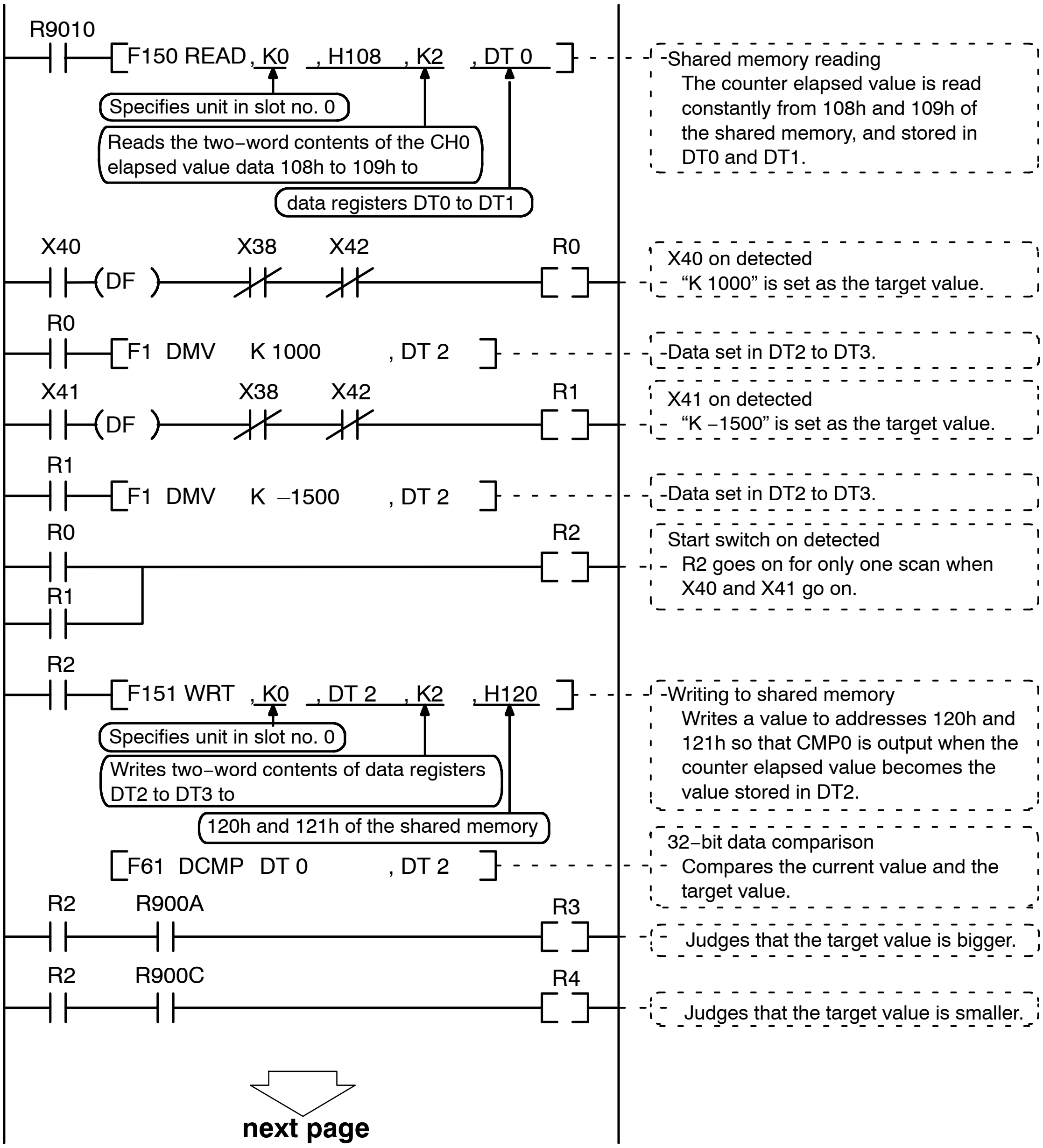
Setting of shared memory addresses 104h and 105h

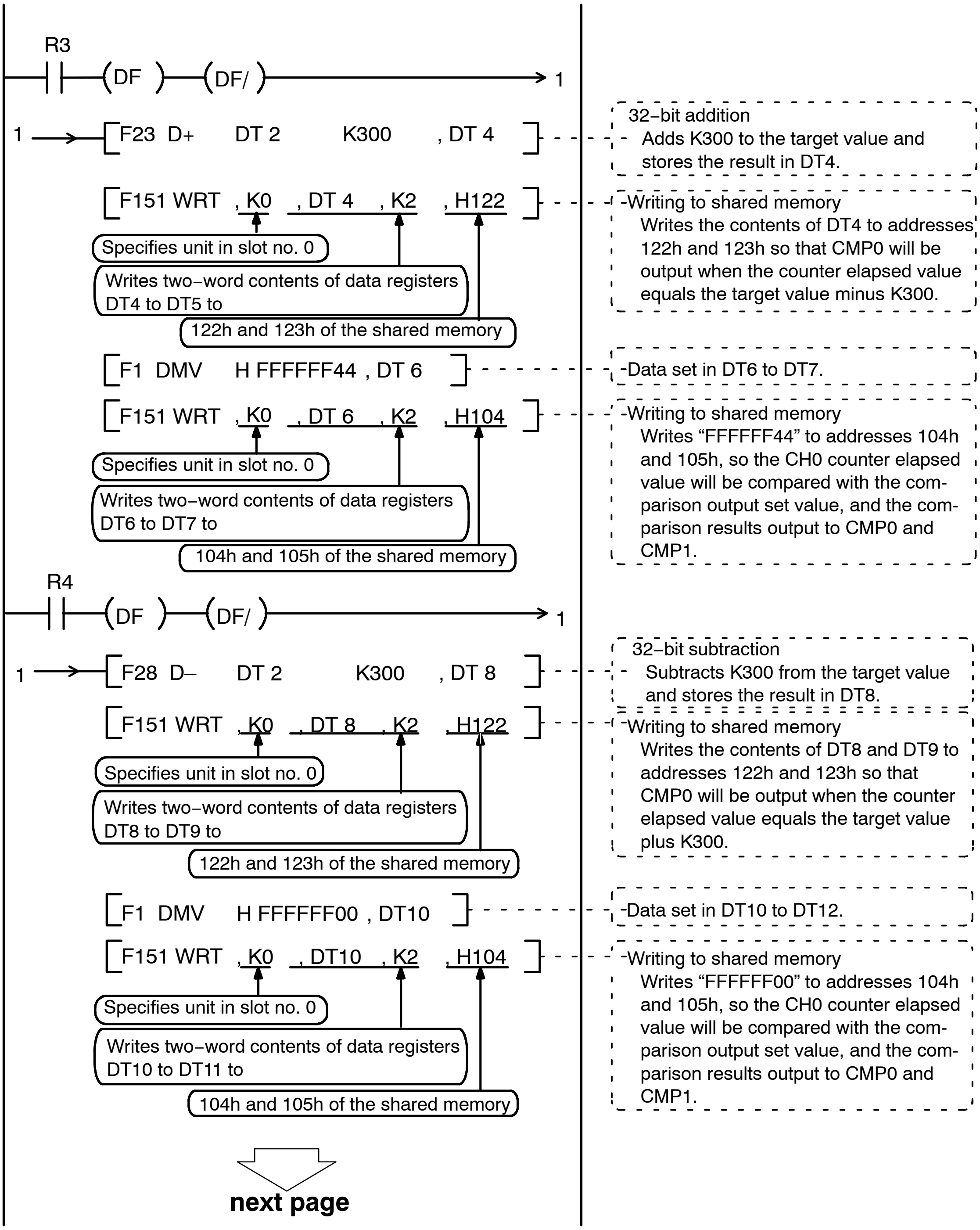
(bit)	32			16	15			0
Comparison output	CMP7	CMP6	CMP5	CMP4	CMP3	CMP2	CMP1	CMP0
Set value (HEX)	F	F	F	F	F	F	4	4
Setting contents (Function)	Not used	Not used	Not used	Not used	Not used	Not used	CH0 comparison*	CH0 comparison*

* Goes on if the elapsed value is more than or equal to the set value

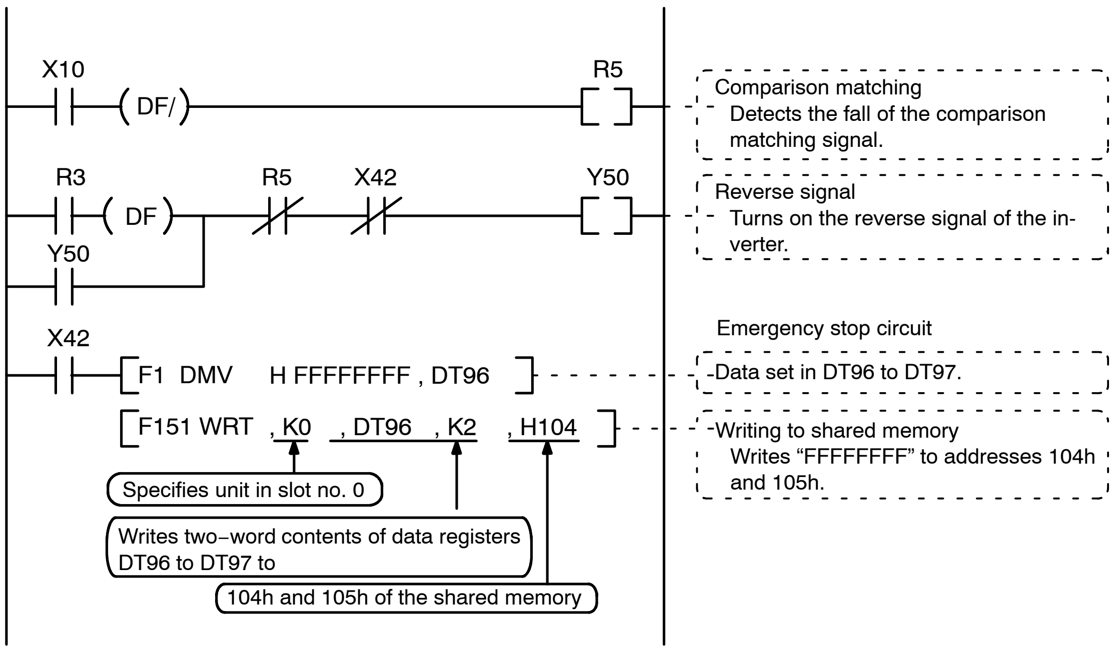
12.3.6 Sample Programs

This program enters settings relating to the counter and comparison functions, and settings relating to pushbutton operation, in the shared memory.




R3
DF
DF/
1
1
F23 D+ DT 2 K300 , DT 4
32−bit addition
Adds K300 to the target value and stores the result in DT4.
F151 WRT , K0 , DT 4 , K2 , H122
Specifies unit in slot no. 0
Writes two−word contents of data registers DT4 to DT5 to
122h and 123h of the shared memory
Writing to shared memory
Writes the contents of DT4 to addresses 122h and 123h so that CMP0 will be output when the counter elapsed value equals the target value minus K300.
F1 DMV H FFFFFF44 , DT 6
Data set in DT6 to DT7.
F151 WRT , K0 , DT 6 , K2 , H104
Specifies unit in slot no. 0
Writes two−word contents of data registers DT6 to DT7 to
104h and 105h of the shared memory
Writing to shared memory
Writes “FFFFFF44” to addresses 104h and 105h, so the CH0 counter elapsed value will be compared with the com-parison output set value, and the com-parison results output to CMP0 and CMP1.
R4
DF
DF/
1
1
F28 D− DT 2 K300 , DT 8
32−bit subtraction
Subtracts K300 from the target value and stores the result in DT8.
F151 WRT , K0 , DT 8 , K2 , H122
Specifies unit in slot no. 0
Writes two−word contents of data registers DT8 to DT9 to
122h and 123h of the shared memory
Writing to shared memory
Writes the contents of DT8 and DT9 to addresses 122h and 123h so that CMP0 will be output when the counter elapsed value equals the target value plus K300.
F1 DMV H FFFFFF00 , DT10
Data set in DT10 to DT12.
F151 WRT , K0 , DT10 , K2 , H104
Specifies unit in slot no. 0
Writes two−word contents of data registers DT10 to DT11 to
104h and 105h of the shared memory
Writing to shared memory
Writes “FFFFFF00” to addresses 104h and 105h, so the CH0 counter elapsed value will be compared with the com-parison output set value, and the com-parison results output to CMP0 and CMP1.
next page

12.3 Position Control Using Absolute Values

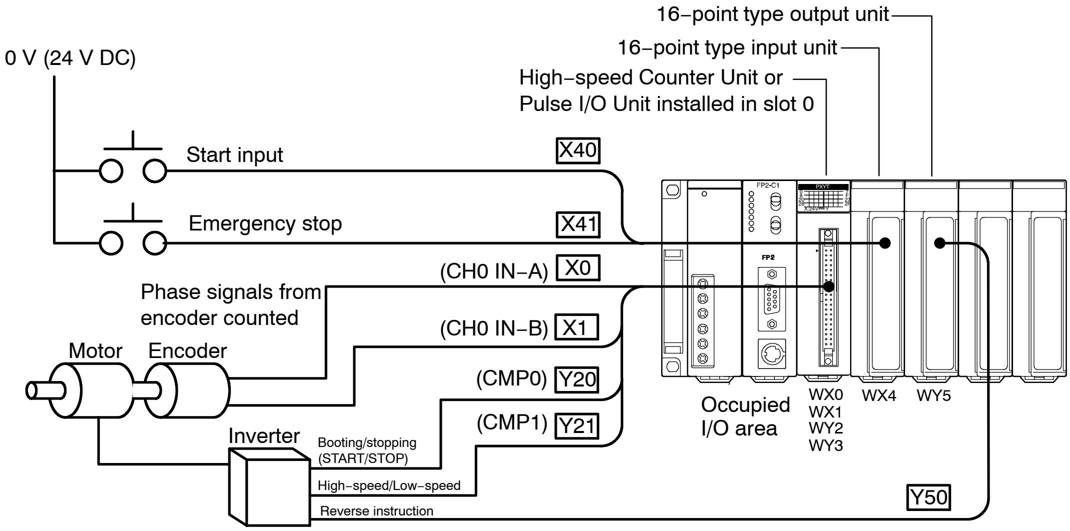


Values stored in data registers

Address	Content
DT0, DT1	Current value (elapsed value)
DT2, DT3	Target value
DT4, DT5	Deceleration point
DT8, DT9	Deceleration point

12.4 Position Control Using Data Tables

12.4.1 Overveiw



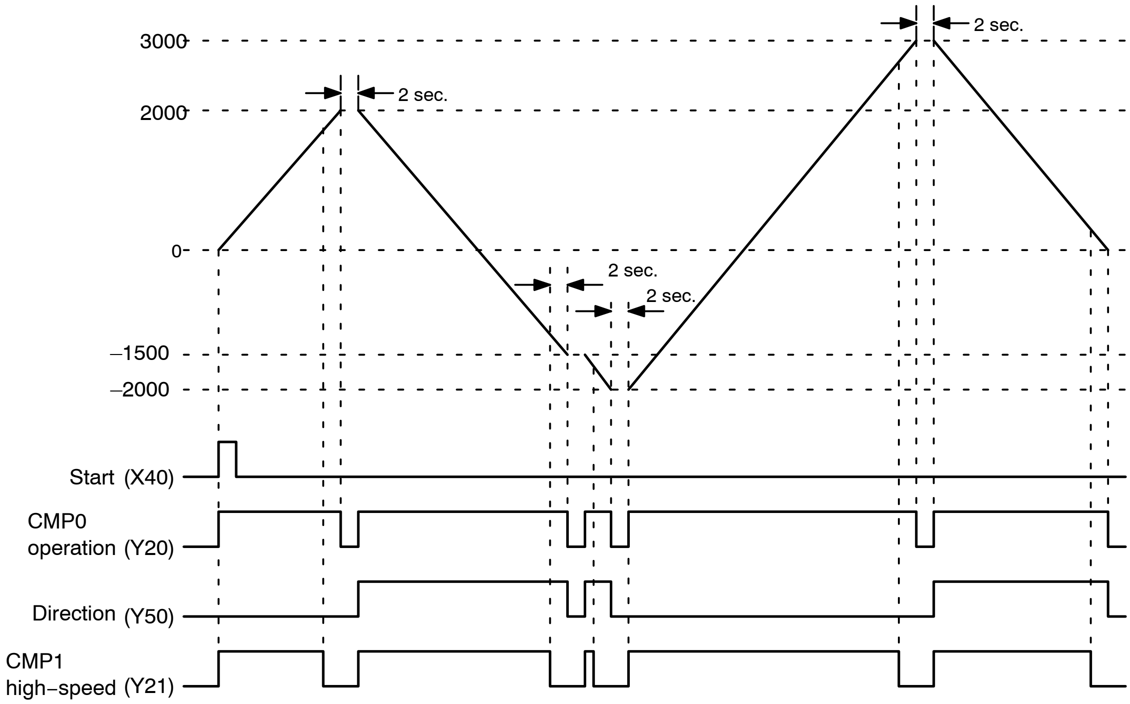
In the example shown here, absolute values are used for positioning control, in accordance with set values that have been set in a data table ahead of time. The speed decreases 300 pulses before the stopping position, and the system then stops.
The data table is created as shown below, and deceleration points (relative pulse values) are registered.

Address	Set value	Content
DT10, DT11	K 300	Speed switching point
DT12, DT13	K 2000	Target value 1
DT14, DT15	K –1500	Target value 2
DT16, DT17	K –2000	Target value 3
DT18, DT19	K 3000	Target value 4
DT20, DT21	K 0	Target value 5

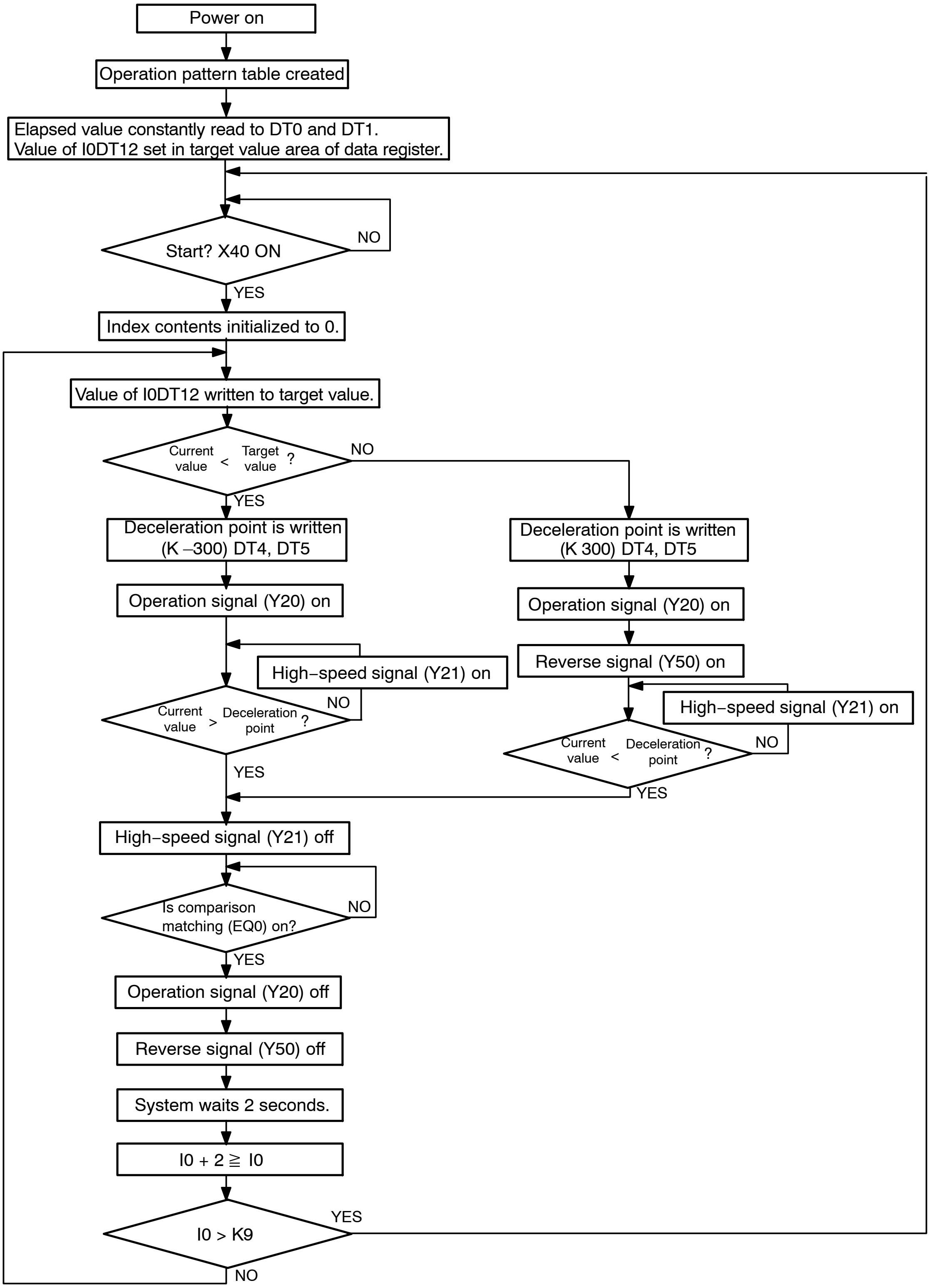
Also, rather than pulse output being used, the inverter is started and stopped using the CMP0 signal, and the CMP1 signal is used for high/low speed control.

12.4.2 Timing Chart

The following shows changes in the count value and output that occur in response to the input statuses of the various signals.
The speed decreases at K 300 pulses before each of the target values.



12.4.3 Flowchart



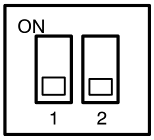
Tip

The phase differential input mode has a multiplier function that can be used to change the multiplication ratio of the input pulses.
For detailed information, see page 1 – 9.

12.4.4 Setting the Mode Setting Switches

Specify “Mode A” to use only the counter function, without using interrupts.

Mode A (SW1 → off, SW2 → off)



No interruption

When this setting is used, the interrupt function will not operate even if used.

The counter function can be used regardless of whether the interrupt function is set to “Used” or “Not Used”.

12.4.5 Shared Memory Settings

Counter Setting

This sets the operation modes for each counter channels.
In this example, phase signals such as encoders are input to X0 and X1, and the counter function is used with the multiplication phase input mode.
Therefore, a value of “FFFFFF20” should be written to addresses 100h and 101h of the shared memory.

Setting of shared memory addresses 100h and 101h

(bit)	32			16	15			0
External input	XD	XC	X9	X8	X5	X4	X1	X0
Counter number	CH3		CH2		CH1		CH0	
Setting item	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting	Input mode	Function setting
Set value	F	F	F	F	F	F	2	0
Setting contents (Function)	Not used	Not used	Not used	Not used	Not used	Not used	Phase input	Terminal input

Setting the Comparison Output Set Value

Here, the comparison output set value, which is compared to the counter elapsed value, is set.
In the example shown here, the values “K 2000 (H 7D0)”, “K –1500 (H FFFFFA24)”, “K –2000 (H FFFFF830)”, “K 3000 (H BB8)”, and “K 0 (H 0)” are sequentially written to addresses 120h and 121h of the shared memory, in accordance with the data table values.

Setting of shared memory addresses 120h and 121h

Target value 1

(bit)	32			16	15			0
Setting item	Comparison output set value (for CMP0)							
Set value (HEX)	0	0	0	0	0	2	D	0
Setting contents (Decimal)	K 2000							

Target value 2

(bit)	32			16	15			0
Setting item	Comparison output set value (for CMP0)							
Set value (HEX)	F	F	F	F	F	A	2	4
Setting contents (Decimal)	K –1500							

☛ next page

Target value 3

(bit)	32			16	15			0
Setting item	Comparison output set value (for CMP0)							
Set value (HEX)	F	F	F	F	F	8	3	0
Setting contents (Decimal)	K –2000							

Target value 4

(bit)	32			16	15			0
Setting item	Comparison output set value (for CMP0)							
Set value (HEX)	0	0	0	0	0	B	B	8
Setting contents (Decimal)	K 3000							

Target value 5

(bit)	32			16	15			0
Setting item	Comparison output set value (for CMP0)							
Set value (HEX)	0	0	0	0	0	0	0	0
Setting contents (Decimal)	K 0							

Comparison Output Setting

The channel number and output logic for the counter used in the comparison output function are selected.

In the example shown here, the counter elapsed value for CH0 is compared with the comparison output set value and the comparison results are output to CMP0 and CMP1.

Write “FFFFFF44” or “FFFFFF00” to addresses 104h and 105h of the shared memory.

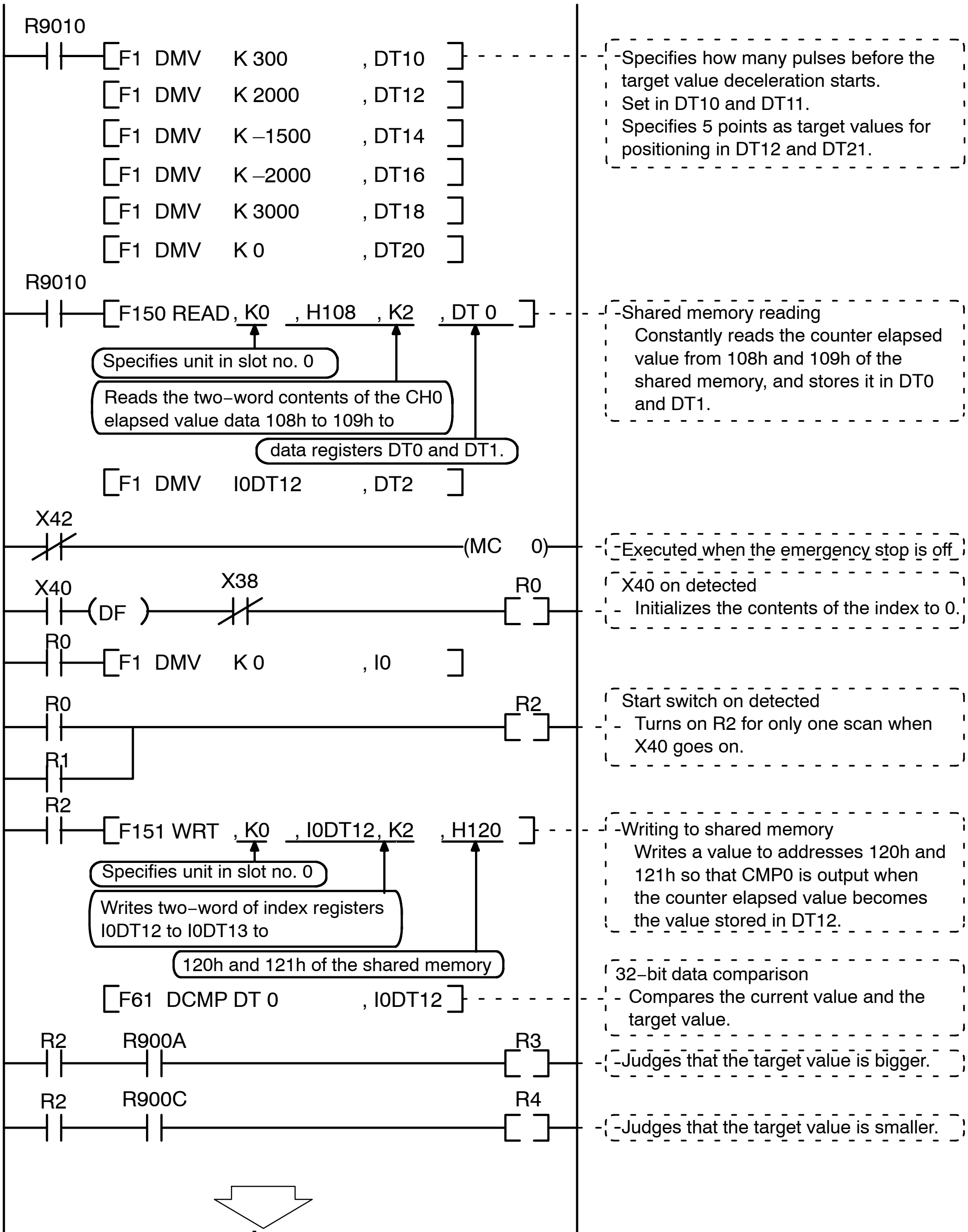
Setting of shared memory addresses 104h and 105h

(bit)	32			16	15			0
Comparison input	CMP7	CMP6	CMP5	CMP4	CMP3	CMP2	CMP1	CMP0
Set value	F	F	F	F	F	F	4	4
Setting contents (Function)	Not used	Not used	Not used	Not used	Not used	Not used	CH0 compari-son*	CH0 compari-son*

* Goes on if the elapsed value is more than or equal to the set value

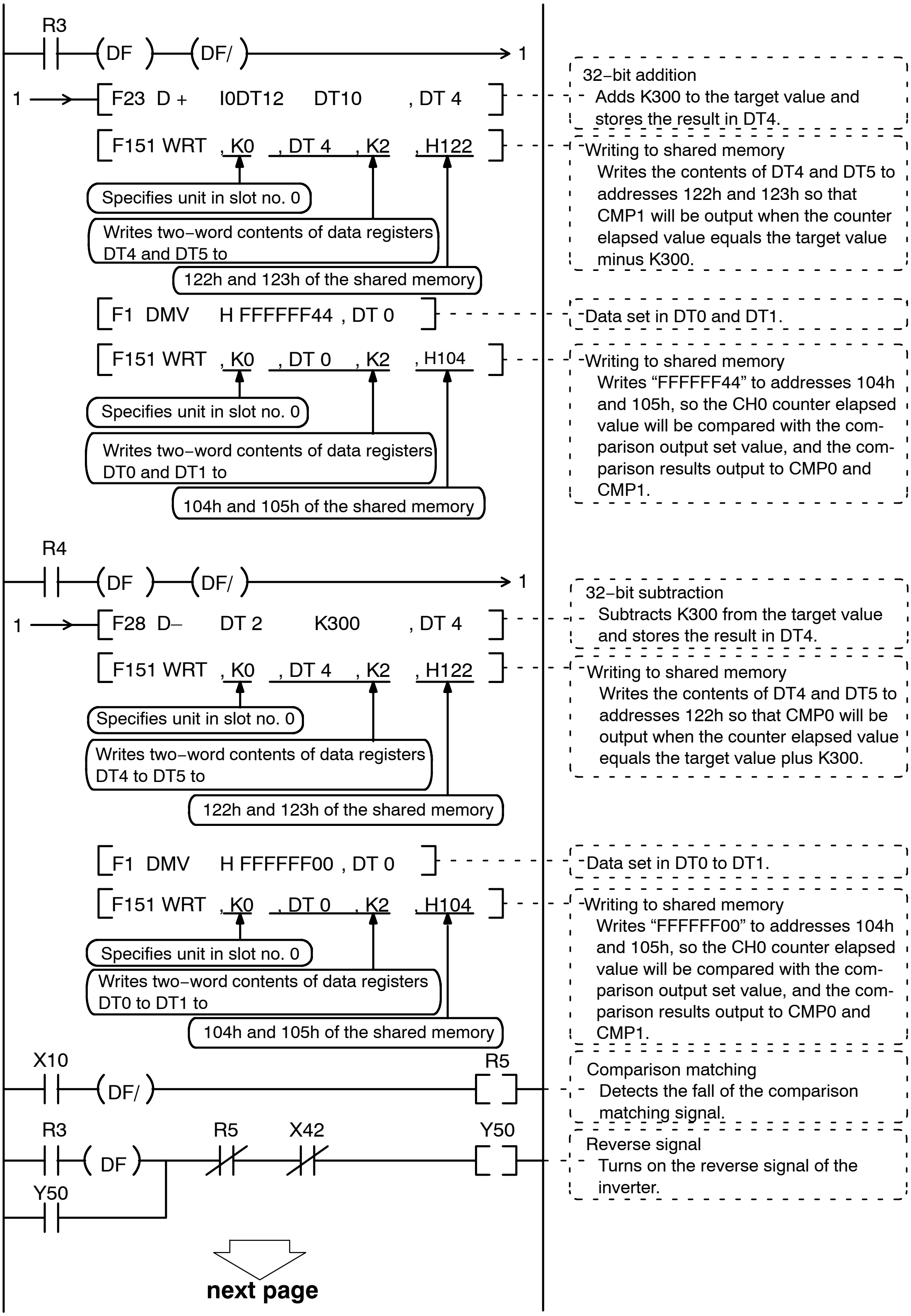
12.4.6 Sample Programs

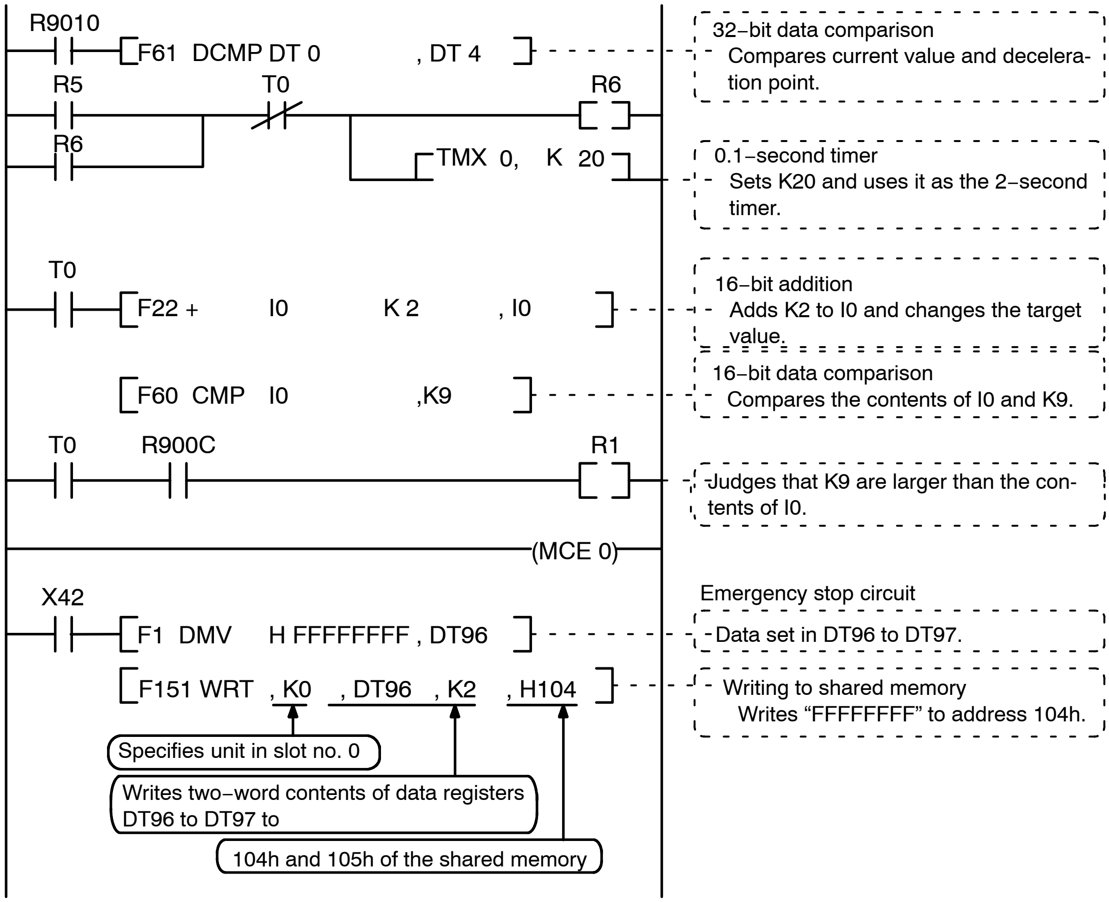
This program enters settings relating to the counter and comparison functions, and settings relating to pushbutton operation, in the shared memory.



next page

12.4 Position Control Using Data Tables





Contents of values stored in data registers

Address	Content
DT0, DT1	Current value (elapsed value)
DT2, DT3	Current target value
DT4, DT5	Deceleration point (Absolute value)
DT10, DT11	Deceleration point (Relative value)

Address	Content
DT12, DT13	Target value 1
DT14, DT15	Target value 2
DT16, DT17	Target value 3
DT18, DT19	Target value 4
DT20, DT21	Target value 5

12.4 Position Control Using Data Tables

Chapter 13

Specifications

13.1 Table of Performance Specifications

General specifications

Item	Specifications
Ambient usage temperature	0 to +55°C/32 to 131°F
Ambient storage temperature	–20 to +70°C/–4 to +158°F
Ambient usage humidity	30 to 85% RH (at 25°C with no condensation)
Ambient storage humidity	30 to 85% RH (at 25°C with no condensation)
Voltage resistance	500 VAC for 1 minute, between DC input/output connector and power supply ground
Insulation resistance	100 M Ω min. between DC input/output connector and power supply ground (test voltage: 500 VDC)
Vibration resistance	10 to 55 Hz sweep/1 minute Duplex amplitude: 0.75 mm, 10 minutes each in X, Y, Z directions
Impact resistance	98 m/s^2, 4 times each in X, Y, Z directions
Noise resistance	1,000 V [p–p], pulse width 50 ns, 1 µs (based on noise simulator)
Usage environment	No corrosive gases, no significant dust.

13.1 Table of Performance Specifications

I/O specifications

Common specifications

Item	FP2 High−speed Counter Unit		FP2 Pulse I/O Unit	
	NPN output	PNP output	NPN output	PNP output
Part No.	FP2−HSCT	FP2−HSCP	FP2−PXYT	FP2−PXYP
No. of dedicated inputs/ outputs	32 inputs, 32 outputs (32SX, 32SY)			
Internal current consumption	450 mA or less (at 5 VDC)		500 mA or less (at 5 VDC)	
Operation display	32−point LED display (lighted when on)			
External connections	Connector connections (One 40P long lever type conforming to MIL standards used)			
Weight	Approx. 110 g/3.9 oz		Approx. 130 g/4.6 oz	

Input specifications

Item			FP2 High−speed Counter Unit		FP2 Pulse I/O Unit	
			NPN output	PNP output	NPN output	PNP output
Part No.			FP2−HSCT	FP2−HSCP	FP2−PXYT	FP2−PXYP
Input	**Insulation method**		Photocoupler insulation			
	Rated input voltage		24 VDC			
	Rated input current		Approx. 7.5 mA (when using 24 VDC)			
	Input impedance		Approx. 3.2 kΩ			
	Usage voltage range		20.4 to 26.4 VDC			
	Min. on voltage/ min. on current		19.2 VDC / 6 mA			
	Max. off voltage/ max. off current		5.0 VDC / 1.5 mA			
	Response time *1	**off → on**	1 μs or less			
		on → off	2 μs or less			
	Input time constant setting		None, 4 μs, 8 μs, 16 μs, 32 μs (set in 2−input units)			
	Common method		16 points/common			
			+ common	− common	+ common	− common
Counter	**No. of counter channels**		4 channels			
	Calculation range		32−bit with sign (–2,147,483,648 to +2,147,483,647)			
	Max. calculation speed *1 *2		200 kHz			
	Input modes		3 modes (direction control, individual input, phase input)			
	Min. input pulse width *1		2.5 μs			
	Other		8 comparison outputs, multiplier function (1, 2, 4)			
Interrupt	**No. of interrupt points *3**		None, 1/unit, 8/unit (set with mode setting switches)			
	Interrupt processing delays		160 μs or less (when using FP2 CPU unit) 50 μs or less (when using FP2SH CPU unit)			

*1: This value is effective when the input time constant (filter) setting is set to “No setting”.

*2: If the quadrupling function is used for counting with phase input, the maximum calculation speed will be 800 kHz.

*3: The number of interrupt points is set using the mode setting switches on the side of the unit. If interrupts are used at a setting of one per unit, the program for interrupts from the external input terminal B1 (X8) or the program for interrupts from comparison 0 (one from among INT16 to INT23) is booted.

Output specifications

<table>
<tr><th colspan="3" rowspan="2">Item</th><th colspan="2">FP2 High−speed Counter Unit</th><th colspan="2">FP2 Pulse I/O Unit</th></tr>
<tr><th>NPN output</th><th>PNP output</th><th>NPN output</th><th>PNP output</th></tr>
<tr><td colspan="3">Part No.</td><td>FP2−HSCT</td><td>FP2−HSCP</td><td>FP2−PXYT</td><td>FP2−PXYP</td></tr>
<tr><td rowspan="12">Output unit specifi-cations</td><td colspan="2">Insulation method</td><td colspan="4">Photocoupler insulation</td></tr>
<tr><td colspan="2">Rated load voltage</td><td colspan="4">5 to 24 VDC</td></tr>
<tr><td colspan="2">Rated load voltage range</td><td colspan="4">4.75 to 26.4 VDC</td></tr>
<tr><td colspan="2">Max. load current</td><td colspan="4">0.1 A (A11 to A18, B11 to B14 pins), 0.8 A (B15 to B18 pins)</td></tr>
<tr><td colspan="2">Leakage current when off</td><td colspan="4">1 μA or less</td></tr>
<tr><td colspan="2">Max. voltage drop when on</td><td colspan="4">0.5 V or less</td></tr>
<tr><td rowspan="2">Response time</td><td>off → on</td><td colspan="4">1 μs or less</td></tr>
<tr><td>on → off</td><td>1 μs or less</td><td>5 μs or less</td><td>1 μs or less</td><td>5 μs or less</td></tr>
<tr><td colspan="2">Surge killer</td><td colspan="4">Zener diode</td></tr>
<tr><td colspan="2">Common method</td><td colspan="4">16 points/common</td></tr>
<tr><td rowspan="2">External power supply</td><td>Voltage</td><td colspan="4">20.4 to 26.4 VDC</td></tr>
<tr><td>Current (at 24 V DC)</td><td>90 mA or less</td><td>200 mA or less</td><td>90 mA or less</td><td>200 mA or less</td></tr>
<tr><td>Counter</td><td colspan="2">Comparison output</td><td colspan="4">8 points (A11 to A18 pins)</td></tr>
<tr><td rowspan="3">Pulse output</td><td colspan="2">Channels</td><td colspan="2" rowspan="7">—</td><td colspan="2">4 channels (B11 to B18 pins)</td></tr>
<tr><td colspan="2">Max. output frequency *1</td><td colspan="2">100 kHz</td></tr>
<tr><td colspan="2">Output modes</td><td colspan="2">2 modes (direction control, individual output)</td></tr>
<tr><td rowspan="4">PWM output</td><td colspan="2">No. of output points</td><td colspan="2">4 channels (B15 to B18 pins)</td></tr>
<tr><td colspan="2">Max. load current</td><td colspan="2">0.8 A</td></tr>
<tr><td colspan="2">Cycle *1</td><td colspan="2">1 Hz to 30 kHz</td></tr>
<tr><td colspan="2">Duty *1</td><td colspan="2">0 to 100% (unit: 1%)</td></tr>
</table>

*1: At maximum load current and resistance load. There may be distortion in the output waveform, depending on the load current and type of load.

Function specifications

Function	Item	FP2 High−speed Counter Unit		FP2 Pulse I/O Unit	
		NPN output (FP2−HSCT)	PNP output (FP2−HSCP)	NPN output (FP2−PXYT)	PNP output (FP2−PXYP)
Input/output	Occupied I/O	32I, 32O			
	No. of external points	16I, 16O			
Interrupts	No. of interrupts	None, 1/unit, 8/unit			
	Modes	No interrupt mode, intelligent unit that produces interrupts, interrupt unit (settings of switches on side of unit)			
Counter	Channels	4 channels			
	Calculation range	32−bit, with sign (–2,147,483,648 to +2,147,483,647)			
	Calculation speed	200 kHz max. *1			
	Input modes	Direction control, individual, phase differential			
	Special functions	Multiplier function (1, 2, 4)			
Comparison output	No. of outputs	8 max.			
Input time constant	No. of points	16 (Unit: 2 points)			
	Constants	4, 8, 16, 32 μs			
Pulse output	Channels	—		4 channels *2	
	Frequency			1 Hz to 100 kHz (setting unit: 1 Hz)	
	Output modes			Direction control, individual output	
PWM	Channels	—		4 channels *2	
	Output current			0.8 A/channel max.	
	Duty			0 to 100% (setting unit: 1%)	
	Cycle			1 Hz to 30 kHz (setting unit: 1 Hz)	

*1: This value is effective when the input time constant (filter) setting is set to “None”.

*2: The same channels are used for pulse output and PWM output. If both functions are being used, the channels to be used for each function are selected as shown in the table below.

Combination	Channel used			
	CH0	CH1	CH2	CH3
1	PWM	PWM	PWM	PWM
2	PLS	PWM	PWM	PWM
3	PLS	PLS	PWM	PWM
4	PLS	PLS	PLS	PWM
5	PLS	PLS	PLS	PLS

13.2 Table of Input/Output Contacts

13.2.1 FP2 High−speed Counter Unit

Input contacts

	External terminal	Function					
		Input	Interrupt	Counter	Comparator	Pulse	PWM
External terminal	A1	X0	—	CH0 IN−A	—	—	—
	A2	X1	—	CH0 IN−B	—	—	—
	A3	X2	—	CH0 Reset	—	—	—
	A4	X3	—	CH0 Mask	—	—	—
	A5	X4	—	CH1 IN−A	—	—	—
	A6	X5	—	CH1 IN−B	—	—	—
	A7	X6	—	CH1 Reset	—	—	—
	A8	X7	—	CH1 Mask	—	—	—
	B1	X8	INT0	CH2 IN−A	—	—	—
	B2	X9	INT1	CH2 IN−B	—	—	—
	B3	XA	INT2	CH2 Reset	—	—	—
	B4	XB	INT3	CH2 Mask	—	—	—
	B5	XC	INT4	CH3 IN−A	—	—	—
	B6	XD	INT5	CH3 IN−B	—	—	—
	B7	XE	INT6	CH3 Reset	—	—	—
	B8	XF	INT7	CH3 Mask	—	—	—
I/Os in the unit	—	X10	—	—	CMP0	—	—
	—	X11	—	—	CMP1	—	—
	—	X12	—	—	CMP2	—	—
	—	X13	—	—	CMP3	—	—
	—	X14	—	—	CMP4	—	—
	—	X15	—	—	CMP5	—	—
	—	X16	—	—	CMP6	—	—
	—	X17	—	—	CMP7	—	—
	—	X18	—	—	—	—	—
	—	X19	—	—	—	—	—
	—	X1A	—	—	—	—	—
	—	X1B	—	—	—	—	—
	—	X1C	—	—	—	—	—
	—	X1D	—	—	—	—	—
	—	X1E	—	—	—	—	—
	—	X1F	—	—	—	—	—

—: No input allocations

Output contacts

	External terminal	Function					
		Output	Interrupt	Counter	Comparator	Pulse	PWM
External terminal	A11	Y20	—	—	[CMP0]	—	—
	A12	Y21	—	—	[CMP1]	—	—
	A13	Y22	—	—	[CMP2]	—	—
	A14	Y23	—	—	[CMP3]	—	—
	A15	Y24	—	—	[CMP4]	—	—
	A16	Y25	—	—	[CMP5]	—	—
	A17	Y26	—	—	[CMP6]	—	—
	A18	Y27	—	—	[CMP7]	—	—
	B11	Y28	—	—	—	—	—
	B12	Y29	—	—	—	—	—
	B13	Y2A	—	—	—	—	—
	B14	Y2B	—	—	—	—	—
	B15	Y2C	—	—	—	—	—
	B16	Y2D	—	—	—	—	—
	B17	Y2E	—	—	—	—	—
	B18	Y2F	—	—	—	—	—
I/Os in the unit	—	Y30	—	CH0 Software reset	—	—	—
	—	Y31	—	CH0 Software mask	—	—	—
	—	Y32	—	CH1 Software reset	—	—	—
	—	Y33	—	CH1 Software mask	—	—	—
	—	Y34	—	CH2 Software reset	—	—	—
	—	Y35	—	CH2 Software mask	—	—	—
	—	Y36	—	CH3 Software reset	—	—	—
	—	Y37	—	CH3 Software mask	—	—	—
	—	Y38	—	—	—	—	—
	—	Y39	—	—	—	—	—
	—	Y3A	—	—	—	—	—
	—	Y3B	—	—	—	—	—
	—	Y3C	—	—	—	—	—
	—	Y3D	—	—	—	—	—
	—	Y3E	—	—	—	—	—
	—	Y3F	—	—	—	—	—

—: No output allocations

[ ]: This is a signal output directly to the I/O connector, and has no relation to the output (Y). However, the status of these signals can be monitored using the input (X) of the same name.

☞ Notes

- **The I/O numbers are for when FP2 High−speed Counter Unit is installed in slot 0. The I/O numbers will change depending on the installation slot.**
- **With the high−speed counter there is no I/O allocation for pulse output or PWM output.**

13.2.2 FP2 Pulse I/O Unit

Input contacts

	External terminal	Function					
		Input	Interrupt	Counter	Comparator	Pulse	PWM
External terminal	A1	X0	—	CH0 IN–A	—	—	—
	A2	X1	—	CH0 IN–B	—	—	—
	A3	X2	—	CH0 Reset	—	—	—
	A4	X3	—	CH0 Mask	—	—	—
	A5	X4	—	CH1 IN–A	—	—	—
	A6	X5	—	CH1 IN–B	—	—	—
	A7	X6	—	CH1 Reset	—	—	—
	A8	X7	—	CH1 Mask	—	—	—
	B1	X8	INT0	CH2 IN–A	—	—	—
	B2	X9	INT1	CH2 IN–B	—	—	—
	B3	XA	INT2	CH2 Reset	—	—	—
	B4	XB	INT3	CH2 Mask	—	—	—
	B5	XC	INT4	CH3 IN–A	—	—	—
	B6	XD	INT5	CH3 IN–B	—	—	—
	B7	XE	INT6	CH3 Reset	—	—	—
	B8	XF	INT7	CH3 Mask	—	—	—
I/Os in the unit	—	X10	—	—	CMP0	—	—
	—	X11	—	—	CMP1	—	—
	—	X12	—	—	CMP2	—	—
	—	X13	—	—	CMP3	—	—
	—	X14	—	—	CMP4	—	—
	—	X15	—	—	CMP5	—	—
	—	X16	—	—	CMP6	—	—
	—	X17	—	—	CMP7	—	—
	—	X18	—	—	—	PLS0 A	—
	—	X19	—	—	—	PLS0 B	—
	—	X1A	—	—	—	PLS1 A	—
	—	X1B	—	—	—	PLS1 B	—
	—	X1C	—	—	—	PLS2 A	PWM0
	—	X1D	—	—	—	PLS2 B	PWM1
	—	X1E	—	—	—	PLS3 A	PWM2
	—	X1F	—	—	—	PLS3 B	PWM3

—: No input allocations

Output contacts

	External terminal	Function					
		Output	Interrupt	Counter	Comparator	Pulse	PWM
External terminal	A11	Y20	—	—	CMP0	PLS0 Direction	—
	A12	Y21	—	—	CMP1	PLS1 Direction	—
	A13	Y22	—	—	CMP2	PLS2 Direction	—
	A14	Y23	—	—	CMP3	PLS3 Direction	—
	A15	Y24	—	—	CMP4	—	—
	A16	Y25	—	—	CMP5	—	—
	A17	Y26	—	—	CMP6	—	—
	A18	Y27	—	—	CMP7	—	—
	B11	Y28	—	—	—	[PLS0 A]	—
	B12	Y29	—	—	—	[PLS0 B]	—
	B13	Y2A	—	—	—	[PLS1 A]	—
	B14	Y2B	—	—	—	[PLS1 B]	—
	B15	Y2C	—	—	—	[PLS2 A]	[PWM0]
	B16	Y2D	—	—	—	[PLS2 B]	[PWM1]
	B17	Y2E	—	—	—	[PLS3 A]	[PWM2]
	B18	Y2F	—	—	—	[PLS3 B]	[PWM3]
I/Os in the unit	—	Y30	—	CH0 Software reset	—	—	—
	—	Y31	—	CH0 Software mask	—	—	—
	—	Y32	—	CH1 Software reset	—	—	—
	—	Y33	—	CH1 Software mask	—	—	—
	—	Y34	—	CH2 Software reset	—	—	—
	—	Y35	—	CH2 Software mask	—	—	—
	—	Y36	—	CH3 Software reset	—	—	—
	—	Y37	—	CH3 Software mask	—	—	—
	—	Y38	—	—	—	PLS0 Enable	PWM0 Enable
	—	Y39	—	—	—	PLS1 Enable	PWM1 Enable
	—	Y3A	—	—	—	PLS2 Enable	PWM2 Enable
	—	Y3B	—	—	—	PLS3 Enable	PWM3 Enable
	—	Y3C	—	—	—	PLS0 Start	PWM0 Start
	—	Y3D	—	—	—	PLS1 Start	PWM1 Start
	—	Y3E	—	—	—	PLS2 Start	PWM2 Start
	—	Y3F	—	—	—	PLS3 Start	PWM3 Start

—: No output allocations

[ ]: This is a signal output directly to the I/O connector, and has no relation to the output (Y). However, the status of these signals can be monitored using the input (X) of the same name.

Note

The I/O numbers in the above chart are for when FP2 Pulse I/O Unit is installed in slot 0. The I/O numbers will change depending on the installation slot.

13.3 Table of Shared Memory Areas

The following shows a map of the shared memory in the FP2 High−speed Counter Unit and FP2 Pulse I/O Unit.

Shared memory map

Address	Address unit (Word)	Function	R/W	Default value (hex) bit31 – bit0	Contents
100h, 101h	2W	Counter setting	R/W	0F0F0F0F	Counter function setting
102h, 103h	2W	Reserved area	—	—	—
104h, 105h	2W	Comparison output setting	—	FFFFFFFF	Comparison output setting
106h, 107h	2W	Reserved area	—	—	—
108h, 109h	2W	Counter (CH0) elapsed value	R/W	00000000	CH0 count elapsed value, 32−bit with sign
10Ah, 10Bh	2W	Counter (CH1) elapsed value	R/W	00000000	CH1 count elapsed value, 32−bit with sign
10Ch, 10Dh	2W	Counter (CH2) elapsed value	R/W	00000000	CH2 count elapsed value, 32−bit with sign
10Eh, 10Fh	2W	Counter (CH3) elapsed value	R/W	00000000	CH3 count elapsed value, 32−bit with sign
110h to 11Fh	2W	Reserved area	—	—	—
120h, 121h	2W	Comparison output set value MEM0	R/W	00000000	Comparison with counter elapsed value, 32−bit with sign
122h, 123h	2W	Comparison output set value MEM1	R/W	00000000	Comparison with counter elapsed value, 32−bit with sign
124h, 125h	2W	Comparison output set value MEM2	R/W	00000000	Comparison with counter elapsed value, 32−bit with sign
126h, 127h	2W	Comparison output set value MEM3	R/W	00000000	Comparison with counter elapsed value, 32−bit with sign
128h, 129h	2W	Comparison output set value MEM4	R/W	00000000	Comparison with counter elapsed value, 32−bit with sign
12Ah, 12Bh	2W	Comparison output set value MEM5	R/W	00000000	Comparison with counter elapsed value, 32−bit with sign
12Ch, 12Dh	2W	Comparison output set value MEM6	R/W	00000000	Comparison with counter elapsed value, 32−bit with sign
12Eh, 12Fh	2W	Comparison output set value MEM7	R/W	00000000	Comparison with counter elapsed value, 32−bit with sign
130h to 137h	2W	Reserved area	—	—	—
138h, 139h	2W	Interrupt setting	R/W	FFFFFFFF	Setting of interrupt input destination
13Ah, 13Bh	2W	Reserved area	—	—	—
13Ch, 13Dh	2W	Input time constant setting	R/W	FFFFFFFF	Input time constant setting up to input X0 to XF
13Eh, 13Fh	2W	Reserved area	—	—	—

R/W: Both reading and writing are possible.
R: Only reading is possible.

☛ next page

Address	Address unit [Word]	Function	R/W	Default value (hex) bit31 – bit0	Contents
140h, 141h	2W	PLS/PWM setting	R/W	FFFFFFFF	Pulse output type setting
142h, 143h	2W	PLS/PWM flag	R	14141414	Monitoring of pulse output status
144h to 147h	2W	Reserved area	—	—	—
148h, 149h	2W	PLS0/PWM0 frequency setting	R/W	00000000	Output frequency setting
14Ah, 14Bh	2W	PLS1/PWM1 frequency setting	R/W	00000000	Output frequency setting
14Ch, 14Dh	2W	PLS2/PWM2 frequency setting	R/W	00000000	Output frequency setting
14Eh, 14Fh	2W	PLS3/PWM3 frequency setting	R/W	00000000	Output frequency setting
150h to 157h	2W	Reserved area	—	—	—
158h, 159h	2W	PWM0 duty setting	R/W	00000000	PWM duty setting
15Ah, 15Bh	2W	PWM1 duty setting	R/W	00000000	PWM duty setting
15Ch, 15Dh	2W	PWM2 duty setting	R/W	00000000	PWM duty setting
15Eh, 15Fh	2W	PWM3 duty setting	R/W	00000000	PWM duty setting

R/W: Both reading and writing are possible.
R: Only reading is possible.

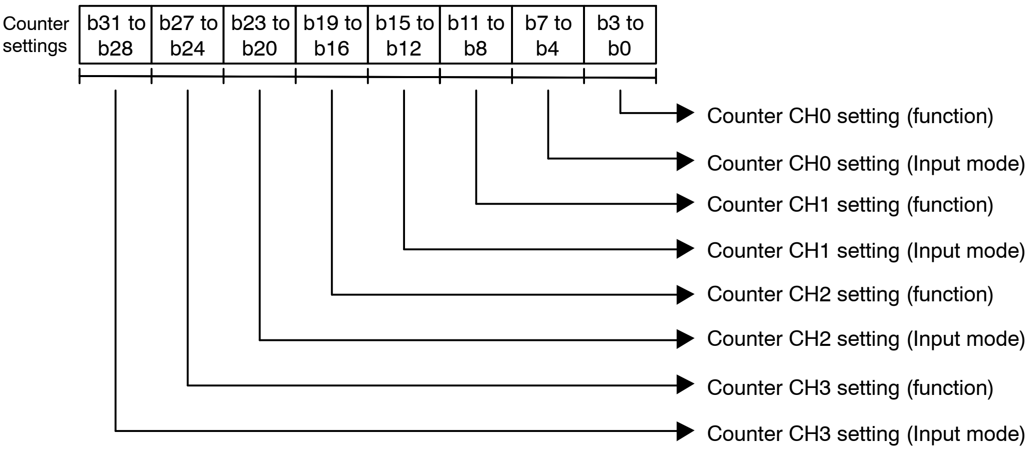
Explanation of shared memory areas

The following indicates the contents of the shared memory in the FP2 High−speed Counter Unit/FP2 Pulse I/O Unit.

100h, 101h	Counter function setting

The settings in the shared memory specify the operation modes for the various counter channels.
The counter function mode settings should be entered as shown below.

Addresses: 100 h, 101h



Settings

Input mode (effective only for terminal input)

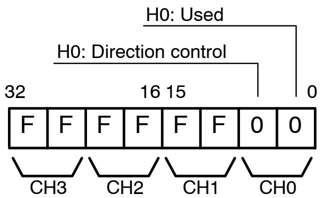
Set value (HEX)	Function	
	Terminal input mode	Multiplier
0	Direction control *3	None
1	Individual input	
2	Phase input	Multiplied once
3		Multiplied twice
4		Multiplied four times
5	Invalid *2	
6		
7		
8		
9		
A		
B		
C		
D		
E		
F		

Functions

Set value (HEX)	Function
	Counter
0	Used (Terminal input)
1	
2	Used (Internal connection) *1
3	
4	Invalid *2
5	
6	
7	
8	
9	
A	
B	
C	
D	
E	
F	Not used *3

*1: Used when pulse output and PWM output are used when an internally connected and the number of pulses output are counted.
*2: This setting should not be used.
*3: When the power supply is turned on, the default setting for the input mode is “Direction control”, and for the function settings is “Not used”.

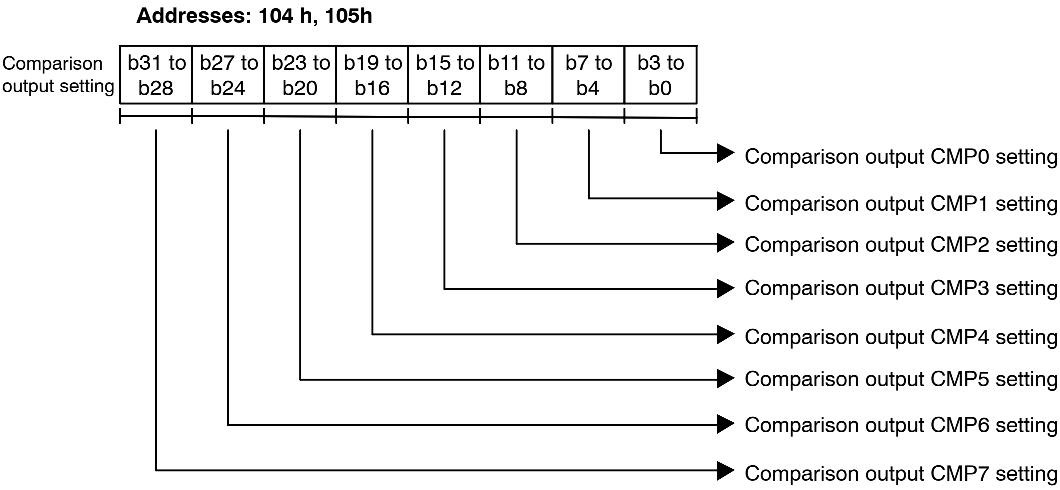
Example of shared memory setting

Setting item	Shared memory no.	Setting example	Setting range
Counter	100h to 101h	8 bits are allocated to each of the channels (CH0 to CH3). 	Setting ranges for the various channels H0: Direction control H10: Individual input H20: Phase input (multiplier: 1) H30: Phase input (multiplier: 2) H40: Phase input (multiplier: 4) HFF: Not used

102h, 103h	Reserved area

104h, 105h	Comparison output setting

Select the counter channel and the output logic used to compare the comparison output set value.

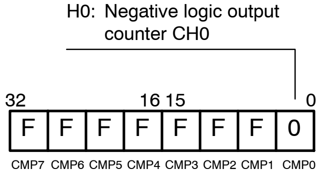


Comparison output setting

Set value (HEX)	Function		
	Comparison output function	Output logic	Counter CH used for comparison
0	Used	on if elapsed value < set value	CH0
1			CH1
2			CH2
3			CH3
4		on if elapsed value ≧ set value	CH0
5			CH1
6			CH2
7			CH3
8	Invalid *1	Invalid *1	
9			
A			
B			
C			
D			
E			
F	Not used *2	—	

*1: No settings should be entered.
*2: When the power supply is turned on, the default value of "Not used" is set for this.

Example of shared memory setting

Setting item	Shared memory no.	Setting example	Setting range
Comparison output setting	104h to 105h	4 bits are allocated to each of the 8 comparison outputs (CMP0 to CMP7).  	Setting ranges for the various comparison outputs On if elapsed value is smaller than set value H0: CH0 H1: CH1 H2: CH2 H3: CH3 On if elapsed value is equal to or larger than set value H4: CH0 H5: CH1 H6: CH2 H7: CH3 HF: Not used

106h, 107h	Reserved area

108h to 10Fh	Counter <CHx> elapsed value

The elapsed values for the various counters are stored in the shared memory.

To read elapsed values, use the F150 (READ) instruction and P150 (PREAD) instruction (these read data from intelligent units), and read the values in two−word units.

	Addresses	Range
Counter CH0 elapsed values	108h, 109h	K–2, 147, 483, 648 to K+2, 147, 483, 647
Counter CH1 elapsed values	10Ah, 10Bh	K–2, 147, 483, 648 to K+2, 147, 483, 647
Counter CH2 elapsed values	10Ch, 10Dh	K–2, 147, 483, 648 to K+2, 147, 483, 647
Counter CH3 elapsed values	10Eh, 10Fh	K–2, 147, 483, 648 to K+2, 147, 483, 647

110h to 11Fh	Reserved area

120h to 12Fh	Comparison output set value

The comparison output set value that is compared against the counter elapsed value must be specified.

Item	Memory	Addresses	Range
Comparison output set value (for CMP0)	MEM0	120h, 121h	K–2, 147, 483, 648 to K+2, 147, 483, 647
Comparison output set value (for CMP1)	MEM1	122h, 123h	K–2, 147, 483, 648 to K+2, 147, 483, 647
Comparison output set value (for CMP2)	MEM2	124h, 125h	K–2, 147, 483, 648 to K+2, 147, 483, 647
Comparison output set value (for CMP3)	MEM3	126h, 127h	K–2, 147, 483, 648 to K+2, 147, 483, 647
Comparison output set value (for CMP4)	MEM4	128h, 129h	K–2, 147, 483, 648 to K+2, 147, 483, 647
Comparison output set value (for CMP5)	MEM5	12Ah, 12Bh	K–2, 147, 483, 648 to K+2, 147, 483, 647
Comparison output set value (for CMP6)	MEM6	12Ch, 12Dh	K–2, 147, 483, 648 to K+2, 147, 483, 647
Comparison output set value (for CMP7)	MEM7	12Eh, 12Fh	K–2, 147, 483, 648 to K+2, 147, 483, 647

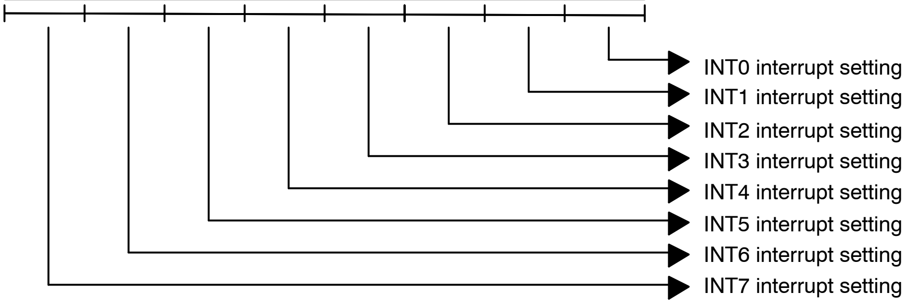
130h to 137h	Reserved area

138h, 139h	Interrupt setting

Set the interrupt function mode as indicated in the table below.

Addresses: 138h, 139h

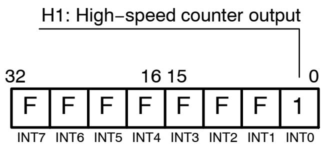
Interrupt setting	b31 to b28	b27 to b24	b23 to b20	b19 to b16	b15 to b12	b11 to b8	b7 to b4	b3 to b0



Set value (HEX)	Function		
	Interrupt function	**Connection destination**	**Interrupt generating conditions**
0	Used	Comparison output function *1 (CMP0 to CMP7)	When output matches
1			
2		Input terminals (X8 to XF)	Off → On
3			On → Off *2
4	Invalid *3	Invalid *3	Invalid *3
5			
6			
7			
8			
9			
A			
B			
C			
D			
E			
F	Not used *4	—	—

*1: INT0 to INT7 correspond to CMP0 to CMP7.
Example: If “Set value 1” is selected for the INT0 interrupt setting, an interrupt is generated if CMP0 matches the output (EQ0).
*2: When this setting has been selected, always execute an interrupt clear command after entering the setting.
*3: No settings should be entered for set values H4 to HE.
*4: When the power supply is turned on, the default value of “Not used” is set for this.

Example of shared memory setting

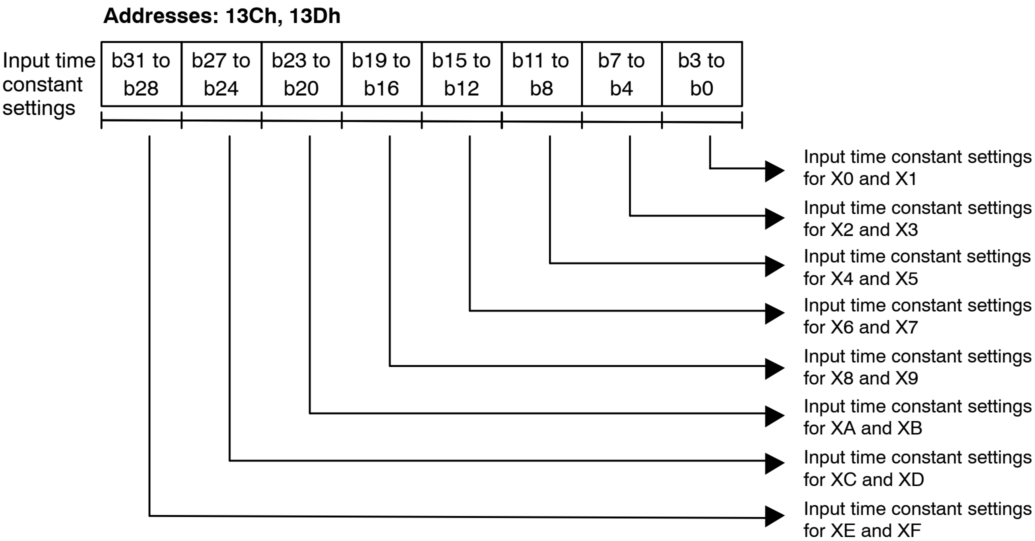
Setting item	Shared memory no.	Setting example	Setting range
Interrupt	138h to 139h	4 bits are allocated to each of the 8 interrupt programs (INT0 to INT7).  	Setting ranges for the various interrupts H1: When high−speed counter output matches H2: When external input goes from off to on H3: When external input goes from on to off HF: Not used

13Ah, 13Bh	Reserved area

13Ch, 13Dh	Input time constant setting

Use the shared memory settings to enter input time constant settings for the group of eight external input terminals.

The input time constants are set for the external input terminals, so the settings for the various function allocations corresponding to inputs X0 to XF also become effective (counter input and interrupt input).



Input time constant settings

Set value (HEX)	Function	
	Input time constant	Effective pulse width
0	Used	4 μs
1		8 μs
2		16 μs
3		32 μs
4	Invalid *1	Invalid *1
5		
6		
7		
8		
9		
A		
B		
C		
D		
E		
F	Not used *2	—

*1: This setting should not be used.
*2: When the power supply is turned on, the default value of “Not used” is set for this.

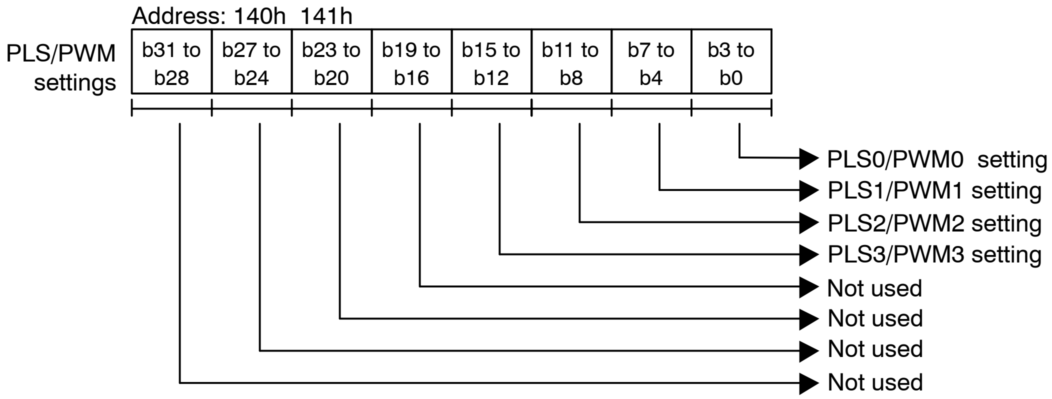
Example of shared memory setting

Setting item	Shared memory no.	Setting example	Setting range
Input time constant	13Ch to 13Dh	4 bits are allocated to each of the 8 interrupt programs (X0, X1 to XE, XF). H2: 16 μs 32 16 15 0 F F F F F F F 2 XF XD XB X9 X7 X5 X3 X1 XE XC XA X8 X6 X4 X2 X0	Setting ranges for the various input time constants H0: 4 μs H1: 8 μs H2: 16 μs H3: 32 μs HF: Not used

13Eh, 13Fh	Reserved area

140h, 141h	PLS/PWM setting

The PWM output type is specified using the PLS/PWM setting in the shared memory.



Pulse output settings (PWM, PLS)

Set value (HEX)	Function		
	Pulse function	**Timing at which data changes**	**Output mode**
0	PWM	Updated at rise of PLSx start signal	—
1		At rise of PLSx start signal, or on comparison output	
2		At rise of PLSx start signal, or when data is updated	
3		Reserved as spare	
4	PLS	Updated at rise of PLSx start signal	Direction control
5			Individual output
6		At rise of PLSx start signal, or on comparison output	Direction control
7			Individual output
8		At rise of PLSx start signal, or when data is updated	Direction control
9			Individual output
A	Invalid *1	Invalid *1	Invalid *1
B			
C			
D			
E			
F	Not used *2	—	—

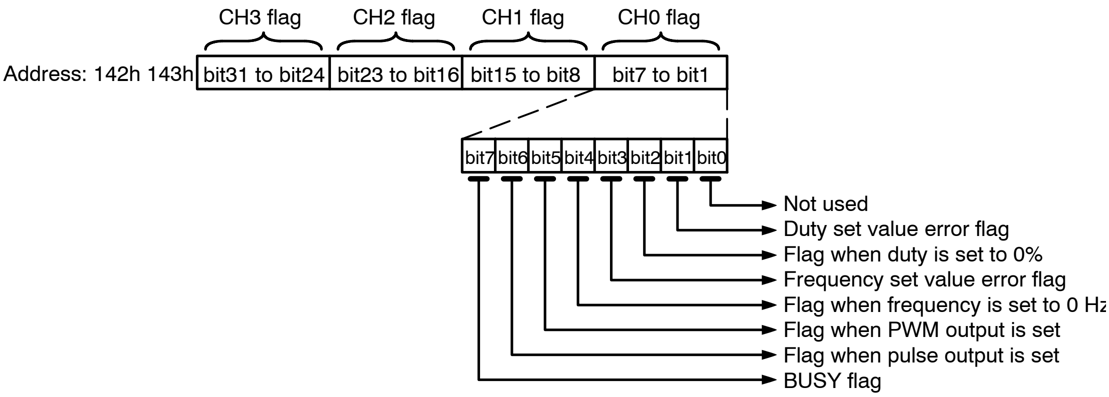
*1: No settings should be entered.
*2: When the power supply is turned on, the default value of “Not used” is set for this.

Example of shared memory setting

Setting item	Shared memory no.	Setting example	Setting range
PLS/PWM setting	140h to 141h	4 bits are allocated to each output (PLS0, PWM0 to PLS3, PWM3). H4: Pulse output (direction control mode) Data updated at rise of Start signal 32 16 15 0 F F F F F F F 4 PLS3 PLS2 PLS1 PLS0 PWM3 PWM2 PWM1 PWM0	Setting ranges for PLS/PWM settings PWM output H0: Data updated at rise of Start signal H1: Data updated at rise of Start signal or on comparison output H2: Data updated at rise of Start signal or when data is refreshed Pulse output (direction control mode) H4: Data updated at rise of Start signal H6: Data updated at rise of Start signal or on comparison output H8: Data updated at rise of Start signal or when data is refreshed Pulse output (individual output mode) H5: Data updated at rise of Start signal H7: Data updated at rise of Start signal or on comparison output H9: Data updated at rise of Start signal or when data is refreshed HF: Not used

142h, 143h	PLS/PWM flag

The status of pulse output can be monitored by reading the status of the bit for this address.



Flag contents

bit 7 . . . . . BUSY flag

This flag indicates that either pulse or PWM output is currently in progress.

1: Output in progress 0: Output is off

bit 6 . . . . . Flag when pulse output is set

This is output when the pulse output function is set.

1: Set 0: Not set

bit 5 . . . . . Flag when PWM output is set

This is output when the PWM output function is set.

1: Set 0: Not set

bit 4 . . . . . Flag when frequency is set to 0 Hz

This is output when the frequency set value has been set to 0 Hz.

1: 0 Hz setting 0: When set to anything other than 0 Hz

bit 3 . . . . . Frequency set value error flag

This is output is a frequency that is higher than the rated frequency settings value is set.

When the PLS output function is being used:

1: 131.072 kHz or higher *1 0: When a value less than that at the left is set

When the PWM output function is being used:

1: 31.458 kHz or higher *1 0: When a value less than that at the left is set

*1: The upper limit for error detection when using the PLS output function is 1048.575 kHz. The upper limit for error detection when using the PWM output function is 41.943 kHz. Setting a value which exceeds either of these prevents normal operation.
For more detailed information, see page 1 – 16.

bit 2 . . . . . Flag when duty is set to 0%

This is output when 0% has been set for the duty set value.

1: 0% setting 0: When anything other than 0% is set

bit 1 . . . . . Duty set value error flag

This is output when a value of 101% or higher has been set for the duty setting value.

1: 101% or higher *2 0: When a value less than that at the left has been set

*2: The upper limit for error detection is 127%. Setting a value which exceeds this prevents normal operation.
For more detailed information, see page 1 – 16.

Flag example

Item		Set value								
		BIN								HEX
		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
When power is turned on		0	0	0	1	0	1	0	0	14
For pulse output	Normal	1	1	0	0	0	1	0	0	C4
	0 Hz setting	1	1	0	1	0	1	0	0	D4
	Frequency set value error	1	1	0	0	1	1	0	0	CC
For PWM output	Normal	1	0	1	0	0	0	0	0	A0
	0 Hz setting	1	0	1	1	0	0	0	0	B0
	Frequency set value error	1	0	1	0	1	0	0	0	A8
	Duty 0% setting	1	0	1	0	0	1	0	0	A4
	Duty set value error	1	0	1	0	0	0	1	0	A2

144h to 147h	Reserved area

148h to 14Fh	PLSx/PWMx frequency setting

	Address	Setting
PLS0/PWM0 frequency setting	148h 149h	For PWM: K0 to K30000
PLS1/PWM1 frequency setting	14Ah 14Bh	For PWM: K0 to K30000
PLS2/PWM2 frequency setting	14Ch 14Dh	For PWM: K0 to K30000
PLS3/PWM3 frequency setting	14Eh 14Fh	For PWM: K0 to K30000

150h to 157h	Reserved area

158h to 15Fh	PWMx duty setting

	Address	Setting
PWM0 Duty setting	158h 159h	K0 to K100
PWM1 Duty setting	15Ah 15Bh	K0 to K100
PWM2 Duty setting	15Ch 15Dh	K0 to K100
PWM3 Duty setting	15Eh 15Fh	K0 to K100

Notes

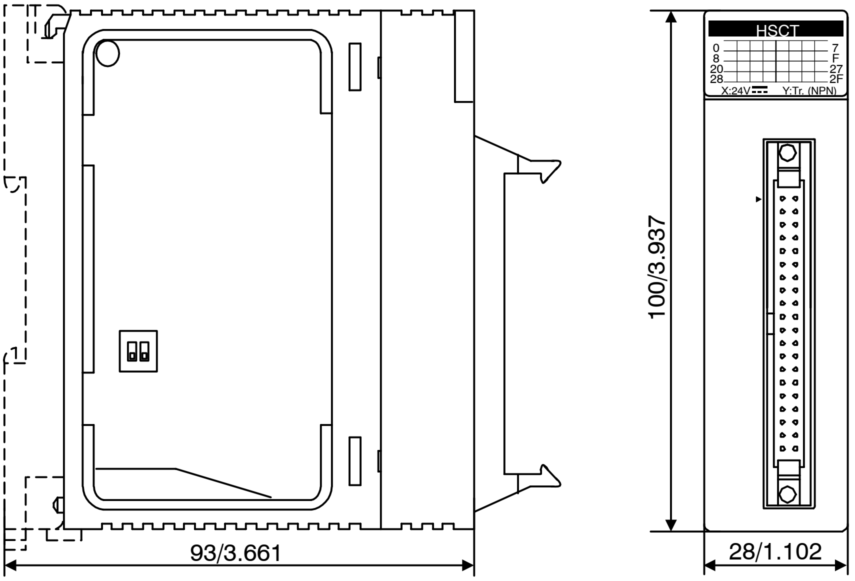
- **If 0 Hz (K0) is set for the PLSx/PWMx frequency, no pulses are output.**
- **The rated values and the error detection ranges for the PLSx/PWMx frequency setting and the PWMx duty setting are as noted below.**
  Be aware that setting a value which exceeds the upper limit for error detection can cause malfunctioning.

Setting		PLS/PWM frequency setting		PWM duty setting	Output pulse
		For PLS function	For PWM function		
Rated value		0 Hz *1 to 100.000 kHz	0 Hz *1 to 30.000 kHz	0% to 100%	Normal output
Other than rated value	Until error is detected	100.001 kHz to 131.071 kHz	30.001kHz to 31.475 khz	—	Normal output *2
	Error detection range	131.072 kHz to 1048.575 kHz	31.485 kHz to 41.943 kHz	101% to 127%	OFF
	Past error detection	1048.576 kHz or more	41.944 kHz or more	127% or more	Normal operation does not take place.

*1: If 0 Hz is set, no pulses are output.
*2: This is affected by the load conditions, and should not be used.

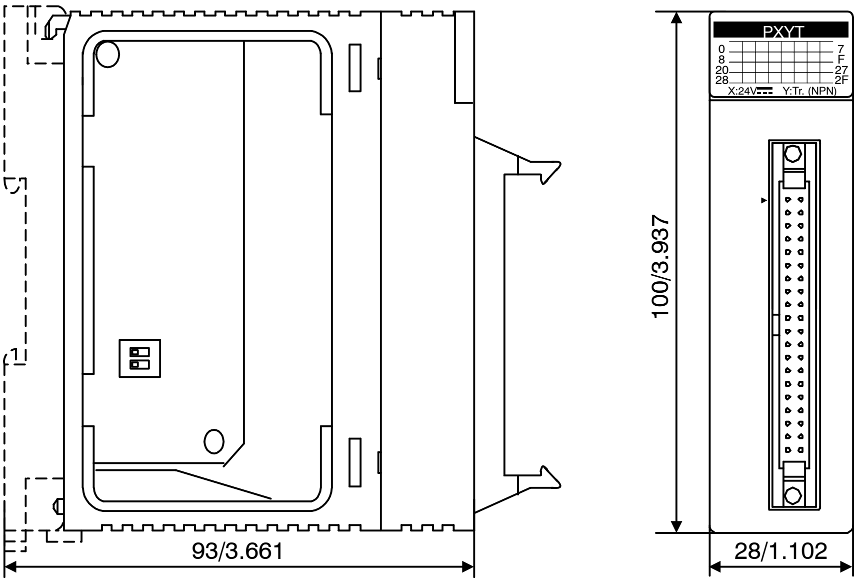
13.4 Dimensions

FP2 High−speed Counter Unit



(unit: mm/in.)

FP2 Pulse I/O Unit



(unit: mm/in.)

Record of changes

Manual No.	Date	Desceiption of changes
ARCT1F323E/ ACG-M323E	JUN.2001	1St Edition
ARCT1F323E-1/ ACG-M323E-1	NOV.2006	2nd Edition
ARCT1F323E-2/ ACG-M323E-2	NOV.2008	3rd Edition
ARCT1F323E-3	AUG.2011	4th Edition - Change in Corporate name - Fixed Errors
ARCT1F323E-4	JUL.2013	5th Edition - Change in Corporate name

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